NANDrive

SST85LD0128 / SST85LD0256 / SST85LD0512

Advance Information

FEATURES:

- **Industry Standard ATA/IDE Bus Interface**
  - Host Interface: 8- or 16-bit access
  - Supports up to PIO Mode-4
  - Supports up to Multi-word DMA Mode-2
- **Low Power, 3.3V Power Supply**
- **5.0V or 3.3V host interface through V_{DDQ} pins**
- **Low current operation:**
  - Active mode: 80 mA Max.
  - Sleep mode: 150 µA Max.
- **Power Management Unit**
  - Immediate disabling of unused circuitry
- **Expanded Data Protection**
  - WP_PD# pin configurable by firmware for prevention of data overwrites
  - Added data security through user-selectable protection zones
- **20-byte Unique ID for Enhanced Security**
  - Factory Pre-programmed 10-byte Unique ID
  - User-Programmable 10-byte ID
- **Integrated Voltage Detector**
  - Industrial Temperature Device requires external POR# signal
- **Endurance**
  - Greater than 100,000 cycles with data wear leveling
- **Data Retention**
  - 10 years
- **Pre-programmed Embedded Firmware**
  - Executes industry standard ATA/IDE commands
  - Implements dynamic wear-leveling algorithms to substantially increase the longevity of flash media
  - Embedded Flash File System
  - Built-in ECC corrects up to 3 random 12-bit symbols of error per 512-byte sector
- **Internal or External System Clock Option**
- **Capacity Expansion Using External Flash Media Devices**
  - Automatic Recognition and Initialization of Flash Media Devices
  - Seamless integration into a standard SMT manufacturing process
- **Multi-tasking Technology enables Fast Sustained Write Performance (Host to Flash)**
  - Up to 8 MB/sec without extended NAND Flash
  - Up to 10 MB/sec with extended NAND Flash
- **Fast Sustained Read Performance (Flash to Host)**
  - Up to 10 MB/sec
- **Commercial and Industrial Temperature Ranges**
  - 0°C to 70°C for commercial operation
  - -40°C to +85°C for industrial operation
- **Industry's smallest 12mm x 18mm LBGA package**
- **All non-Pb (lead-free) devices are RoHS compliant**

PRODUCT DESCRIPTION

The SST85LD0128, SST85LD0256, and SST85LD0512 NANDrive™ integrated circuits (IC) are high-performance, fully-integrated, embedded flash solid state drives. They combines an integrated ATA Controller and a 128/256/512 MB NAND Flash die in a multi-chip package. These products are well suited for solid state mass storage applications offering new and expanded functionality while enabling cost effective designs.

ATA-based solid state mass storage technology is widely used in such products as portable and desktop computers, digital cameras, music players, handheld data collection scanners, cellular phones, PCS phones, PDAs, handy terminals, personal communicators, advanced two-way pagers, audio recorders, monitoring devices, and set-top boxes. SST NANDrive IC supports standard ATA/IDE protocol with up to PIO Mode-4 and Multi-word DMA Mode-2 interface.

The NANDrive is a single device, solid state drive that is designed for embedded systems using standard ATA/IDE protocol. It has built in microcontroller and file management firmware that communicates with ATA standard interfaces; therefore, the device does not require additional or proprietary software such as Flash File System (FFS) and Memory Technology Driver (MTD) software.

The NANDrive provides complete IDE Hard Disk Drive functionality and compatibility in the industry's smallest 12mmx18mm BGA package for easy, space saving, and cost effective mounting to a system motherboard. It is a perfect solution for portable, consumer and OEM, electronic products requiring smaller and more reliable data storage.

The SST85LD0128/0256/0512 NANDrive devices offer added security protection for confidential information stored in the flash media. They allow up to four protection zones which can be set by the user to be Read-only or Hidden (Read-disabled). The SST85LD0128/0256/0512 accesses data within the protected zones through a password-protected command. The NANDrive also provides a WP_PD# pin to protect critical information stored in the flash media from unauthorized overwrites.

The NANDrive devices come pre-programmed with a 10-byte unique serial ID. For even greater system security, the user has the option of programming an additional 10 Bytes of ID space to create a unique, 20-byte ID. Additionally, the capacity of the NANDrive products can be easily expanded by connecting discrete NAND flash components through the external Media bus.

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1.0 GENERAL DESCRIPTION

The SST85LD0128/0256/0512 devices contain an integrated ATA Controller and NAND Flash die in a LBGA package. Refer to Figure 2-1 for the NANDrive block diagram.

1.1 Performance-optimized NANDrive

The heart of the NANDrive is the ATA Flash Disk Controller which translates standard ATA signals into flash media data and control signals. The following components contribute to the NANDrive's operation.

1.1.1 Microcontroller Unit (MCU)

The MCU translates ATA/IDE commands into data and control signals required for flash media operation.

1.1.2 Internal Direct Memory Access (DMA)

The NANDrive uses internal DMA allowing instant data transfer from buffer to flash media. This implementation eliminates microcontroller overhead associated with the traditional, firmware-based approach, thereby increasing the data transfer rate.

1.1.3 Power Management Unit (PMU)

The power management unit controls the power consumption of the NANDrive. The PMU dramatically reduces the power consumption of the NANDrive by putting the part of the circuitry that is not in operation into sleep mode.

1.1.4 SRAM Buffer

A key contributor to the NANDrive performance is an SRAM buffer. The buffer optimizes the host's data transfer to and from the flash media.

1.1.5 Embedded Flash File System

The embedded flash file system is an integral part of the NANDrive. It contains MCU firmware that performs the following tasks:

1. Translates host side signals into flash media writes and reads.
2. Provides dynamic flash media wear leveling to spread the flash writes across all unused memory address space to increase the longevity of flash media.
3. Keeps track of data file structures.
4. Manages system security for the selected protection zones.

1.1.6 Error Correction Code (ECC)

The NANDrive utilizes 72-bit Reed-Solomon Error Detection Code (EDC) and Error Correction Code (ECC), which provides the following error immunity for each 512-byte block of data:

1. Corrects up to three random 12-bit symbol errors.
2. Corrects single bursts up to 25 bits.
3. Detects single bursts up to 61 bits and double bursts up to 15 bits.
4. Detects up to six random 12-bit symbol errors.

1.1.7 Serial Communication Interface (SCI)

The Serial Communication Interface (SCI) is designed for manufacturing error reporting.

1.1.8 Multi-tasking Interface

The multi-tasking interface enables fast, sustained write performance by allowing concurrent Read, Program, and Erase operations to multiple flash media devices.

1.2 NAND Flash

The SST85LD0128/0256/0512 devices utilize standard NAND Flash for data storage.

2.0 FUNCTIONAL BLOCKS

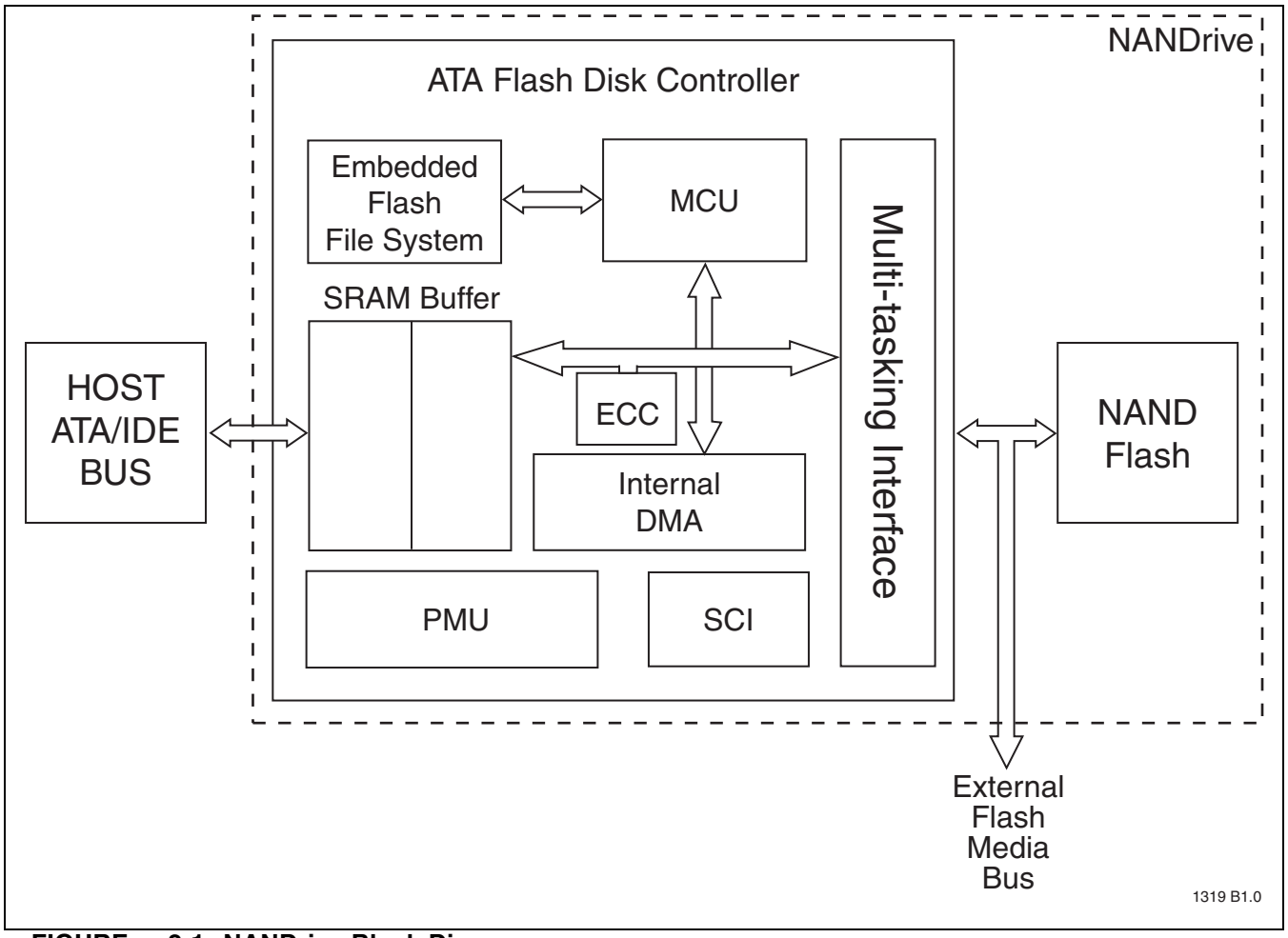

FIGURE 2-1: NANDrive Block Diagram

3.0 PIN ASSIGNMENTS

The signal/pin assignments are listed in Table 3-1. Low active signals have a "#" suffix. Pin types are Input, Output, or Input/Output. Signals whose source is the host are designated as inputs while signals that the NANDrive sources are outputs.

The NANDrive functions in ATA mode, which is compatible with IDE hard disk drives.

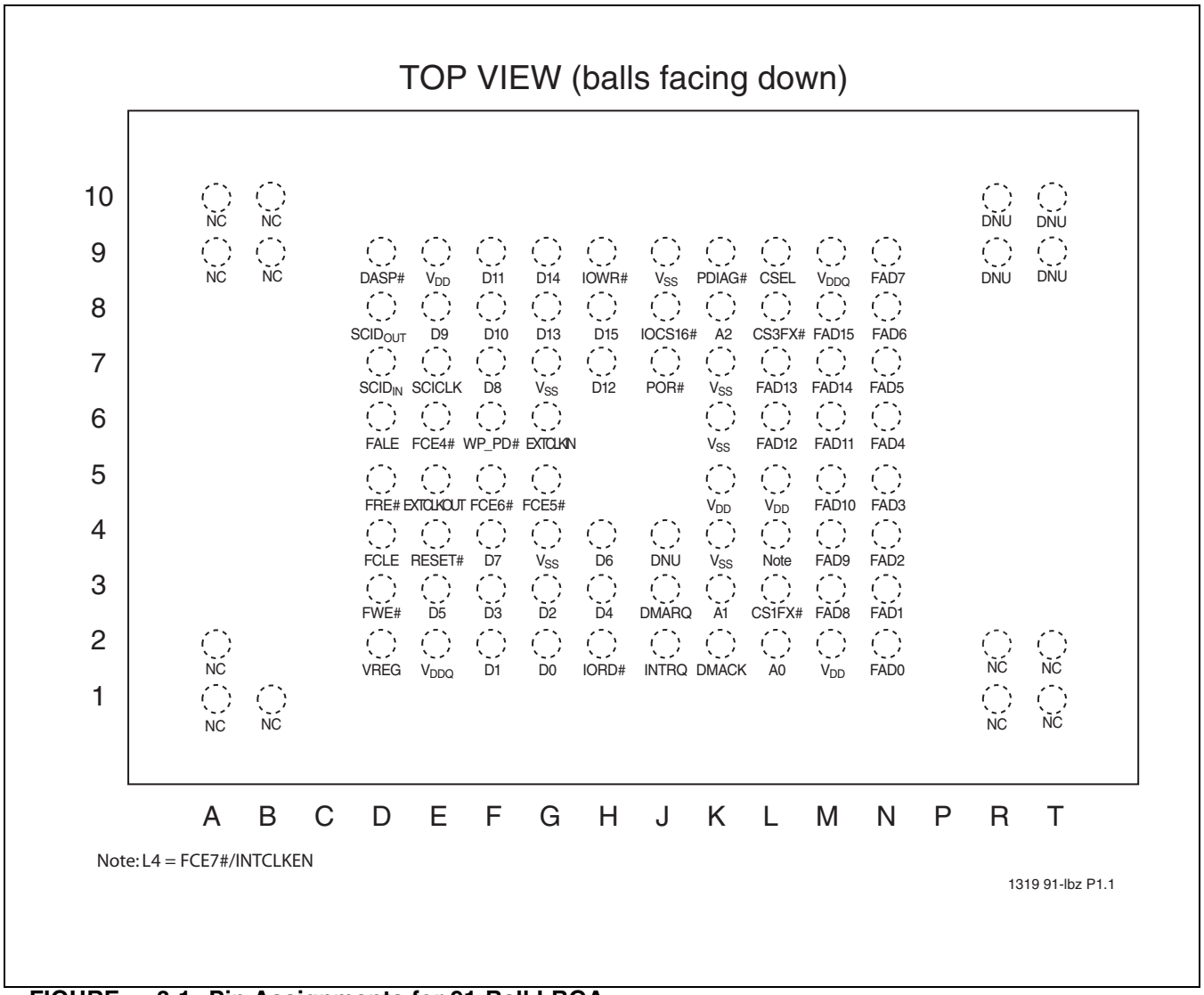

FIGURE 3-1: Pin Assignments for 91-Ball LBGA

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TABLE 3-1: Pin Assignments (1 of 3)

Symbol	Pin No. 91-TFBGA	Pin Type	I/O Type	Name and Functions
Host Side Interface				
A2	K8	I	I1Z	A[2:0] are used to select one of eight registers in the Task File.
A1	K3			
A0	L2			
D15	H8	I/O	I1Z/O2	D[15:0] Data bus
D14	G9			
D13	G8			
D12	H7			
D11	F9			
D10	F8			
D9	E8			
D8	F7			
D7	F4			
D6	H4			
D5	E3			
D4	H3			
D3	F3			
D2	G3			
D1	F2			
D0	G2			
DMACK	K2	I	I2U	DMA Acknowledge - input from host
DMARQ	J3	O	O1	DMA Request to host
CS1FX#	L3	I	I2Z	CS1FX# is the chip select for the task file registers
CS3FX#	L8			CS3FX# is used to select the alternate status register and the Device Control register.
CSEL	L9	I	I1U	This internally pulled-up signal is used to configure this device as a Master or a Slave. When this pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave. The pin setting should remain the same from Power-on to Power-down.
IORD#	H2	I	I2Z	This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the chip.
IOWR#	H9			The I/O Write strobe pulse is used to clock I/O data into the chip.
IOCS16#	J8	O	O2	This output signal is asserted low when the device is indicating a word data transfer cycle.
INTRQ	J2	O	O1	This signal is the active high Interrupt Request to the host.
PDIAG#	K9	I/O	I1U/O1	The Pass Diagnostic signal in the Master/Slave handshake protocol.
DASP#	D9	I/O	I1U/O6	The Drive Active/Slave Present signal in the Master/Slave handshake protocol.
RESET#	E4	I	I2U	This input pin is the active low hardware reset from the host.
WP_PD#	F6	I	I1U	The WP_PD# pin can be used for either the Write Protect mode or Power-down mode, but only one mode is active at any time. The Write Protect or Power-down modes can be selected through the host command. The Write Protect mode is the factory default setting.

TABLE 3-1: Pin Assignments (Continued) (2 of 3)

Symbol	Pin No. 91-TFBGA	Pin Type	I/O Type	Name and Functions
External Flash Media Bus				
FRE#	D5	O	O5	Active Low Flash Media Chip Read
FWE#	D3			Active Low Flash Media Chip Write
FCLE	D4			Active High Flash Media Chip Command Latch Enable
FALE	D6			Active High Flash Media Chip Address Latch Enable
FAD15	M8	I/O	I3U/O5	Flash Media Chip High Byte Address/Data Bus pins
FAD14	M7			
FAD13	L7			
FAD12	L6			
FAD11	M6			
FAD10	M5			
FAD9	M4			
FAD8	M3			
FAD7	N9	I/O	I3U/O5	Flash Media Chip Low Byte Address/Data Bus pins
FAD6	N8			
FAD5	N7			
FAD4	N6			
FAD3	N5			
FAD2	N4			
FAD1	N3			
FAD0	N2			
FCE6#	F5	O	O4	Active Low Flash Media Chip Enable pin
FCE5#	G5			
FCE4#	E6			
FCE7#/ INTCLKEN	L4	I/O	I3D/O4	Active Low Flash Media Chip Enable pin This pin is sensed during the Power-on Reset (POR) to select an internal clock mode. If this pin is pulled up during the Power-on Reset then the internal clock is selected.

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TABLE 3-1: Pin Assignments (Continued) (3 of 3)

Symbol	Pin No. 91-TFBGA	Pin Type	I/O Type	Name and Functions
Serial Communication Interface (SCI)				
$SCID_{OUT}$	D8	O	O4	SCI interface data output
$SCID_{IN}$	D7	I	I3U	SCI interface data input
SCICLK	E7	I	I3U	SCI interface clock
External Clock Option				
FCE7#/ INTCLKEN	L4	I/O	I3D/O4	Active Low Flash Media Chip Enable pin This pin is sensed during the Power-on Reset (POR) to select an Internal Clock mode. If this pin is pulled up during the Power-on Reset then the Internal Clock is selected.
$EXTCLK_{IN}$	G6	I	I4Z	External Clock source input pin
$EXTCLK_{OUT}$	E5	O	O4	External Clock source output pin
Miscellaneous				
V_{SS}	G7, K7, K6, G4, K4, J9	PWR		Ground
V_{DD}	E9, K5, L5, M2	PWR		V_{DD} (3.3V)
V_{DDQ}	M9, E2	PWR		V_{DDQ} (5V/3.3V) for Host interface
POR#	J7	I	Analog Input[1]	Power-on Reset (POR). Active Low
V_{REG}[1]	D2			Capacitor pin, should connect 4.7µ cap to ground for future compatibility.
DNU[2]	J4, R9, R10, T9, T10			Do not use.
NC[3]	A1, A2, A9, A10, B1, B9, B10, R1, R2, T1, T2			No Connect

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1. Analog input for supply voltage detection
2. This pin is a no connect.
3. This pin is a no connect used for mechanical stability.

4.0 CAPACITY SPECIFICATION

Table 4-1 shows the default capacity and specific settings for heads, sectors, and cylinders. The capacities listed apply to either a single device or an externally expanded NANDrive. Users can change the default settings in the drive ID table (see Table 12-4) for customization. If the total number of bytes is less than the default, the remaining space could be used as spares to increase the flash drive endurance. It should also be noted that if the total flash drive capacity exceeds the total default number of bytes, the flash drive endurance will be reduced.

TABLE 4-1: Default NANDrive Settings

Capacity	Total Bytes	Cylinders	Heads	Sectors	Max LBA
128 MB	128,057,344	977	8	32	250,112
256 MB	256,901,120	980	16	32	501,760
512 MB	512,483,328	993	16	63	1,000,944

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TABLE 4-2: Sustained Performance

Product	Write Performance	Read Performance
SST85LD0128	Up to 5 MB/sec without extended NAND Flash Up to 10 MB/sec with extended NAND Flash	Up to 10 MB/sec
SST85LD0256	Up to 5 MB/sec without extended NAND Flash Up to 10 MB/sec with extended NAND Flash	Up to 10 MB/sec
SST85LD0512	Up to 8 MB/sec without extended NAND Flash Up to 10 MB/sec with extended NAND Flash	Up to 10 MB/sec

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5.0 EXTERNAL CLOCK INTERFACE

The external clock interface allows NANDrive operation from an external clock source generated by an RC circuit. Do not use a free running clock as input to the EXTCLKIN pin; an RC circuit must be used. Contact SST for reference circuit and recommended external clock settings.

While the device has an internal clock source, the external clock source allows slowing of the system clock operation to limit the peak current and overcome additional bus loading.

The external clock interface consists of three signals: INTCLKEN, EXTCLKIN, and EXTCLKOUT. The INTCLKEN pin selects between external and internal clock sources for the NANDrive. If this pin is pulled high before device Power-on, then the internal clock source is selected; otherwise, the external clock source is selected. The EXTCLKIN and EXTCLKOUT signals are the input and output clock signals, respectively.

6.0 SECURITY FEATURES

The SST85LD0128 / SST85LD0256 / SST85LD0512 NANDrive devices offer added data protection for applications where data security is of the utmost importance. The secure features are:

1. Protection zones - Customer can enable up to 4 independent protection zones, with two options:
   Read-only or
   Hidden (Read and Write protected) within each protected zone. If protection zones are not enabled the data is unprotected (default configuration).
2. Password protection - Accessing information within the protected zones can be only achieved through a
   customer-unique password.
3. Purge command - The system can issue a Purge command to erase all information stored in the flash media.

Contact SST for detailed specifications.

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7.0 CONFIGURABLE WRITE PROTECT/POWER-DOWN MODES

The WP_PD# pin can be used for either Write Protect mode or Power-down mode, but only one mode is active at any time. Either mode can be selected through the host command, Set-WP_PD#-Mode, explained in Section 12.2.1.31.

Once the mode is set with this command, the device will stay in the configured mode until the next time this command is issued. Power-off or reset will not change the configured mode.

7.1 Write Protect Mode

When the device is configured in the Write Protect mode, the WP_PD# pin offers extended data protection. This feature can be either selected through a jumper or host logic to protect the stored data from inadvertent system writes or erases, and viruses. The Write Protect feature protects the full address space of the data stored on the flash media.

In the Write Protect mode, the WP_PD# pin should be asserted prior to issuing the destructive commands: Erase-Sector, Format-Track, Write-DMA, Write-Long-Sector, Write-Multiple, Write-Multiple-without-Erase, Write-Sector(s), Write-Sector-without-Erase, or Write-Verify. This will force the NANDrive to reject any destructive commands from the ATA interface. All destructive commands will return 51H in the Status register and 04H in the Error register signifying an invalid command. All non-destructive commands will be executed normally.

7.2 Power-down Mode

When the device is configured in the Power-down mode, if the WP_PD# pin is asserted during a command, the NANDrive completes the current command and returns to the standby mode immediately to save power. Afterwards, the device will not accept any other commands. Only a Power-on Reset (POR) or hardware reset will bring the device to normal operation with the WP_PD# pin de-asserted.

8.0 POWER-ON INITIALIZATION AND CAPACITY EXPANSION

NANDrive is self-initialized during the first power-up. As soon as the power is applied to the NANDrive it reports busy for up to five seconds while performing bad blocks search and low level format. This initialization is a one time event.

The NANDrive allows storage capacity expansion by using additional external NAND Flash devices. Contact SST for a list of supported standard NAND flash media devices for each NANDrive product. During the first self-initialization, the NANDrive firmware scans all connected flash media devices and reads their device ID. If the device ID matches the listed flash media devices, the NANDrive performs drive recognition based on the algorithm provided by the flash media suppliers, including setting up the bad block table, executing all the necessary handshaking routines for flash media support, and, finally, performing the low-level format. For Power-on Timing Specifications, please refer to Table 13-2.

9.0 LIFETIME EXPECTANCY

NANDrive provides minimum endurance of 100,000 program/erase cycles and 10 year data retention as stated by the selected NAND Flash components. The extensive ECC and wear leveling algorithms utilized in the NANDrive extend the life of the product. Please refer to Wear Leveling Architecture Technical Paper for real application life time calculation.

If the drive initialization fails, and a visual inspection is unable to determine the problem, SST provides a comprehensive interface for manufacturing flow debug. This interface not only allows debug of the failure and manual reset of the initialization process, but also allows customization of user definable options.

8.1 ATA/IDE Interface

The ATA interface can be used for NANDrive manufacturing support. SST provides an example of a DOS-based solution (an executable routine downloadable from www.sst.com) for manufacturing debug and rework.

8.2 Serial Communication Interface (SCI)

For additional manufacturing flexibility, the SCI bus can be used for manufacturing error reporting. The SCI consists of 3 active signals: SCIDOUT, SCIDIN, and SCICLK.

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10.0 POWER-ON AND BROWN-OUT RESET CHARACTERISTICS

Please contact SST to obtain NANDrive reference design schematics including the POR# circuit for commercial and industrial NANDrive offerings.

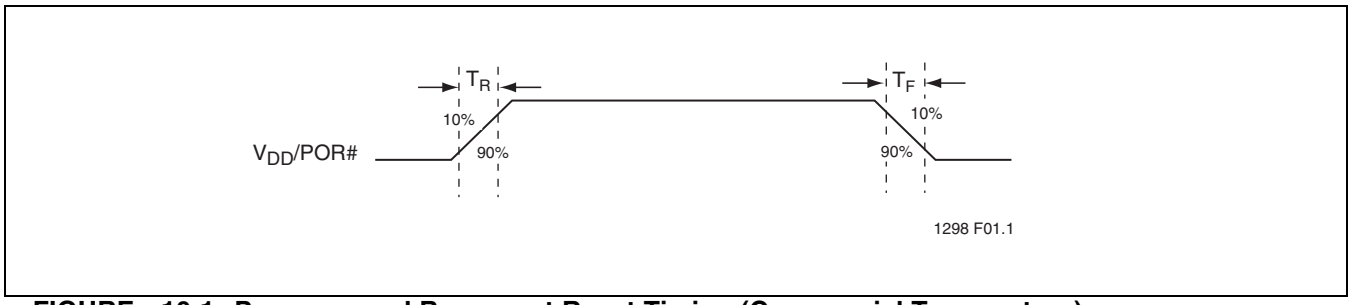

FIGURE 10-1: Power-on and Brown-out Reset Timing (Commercial Temperature)

TABLE 10-1: Power-on and Brown-out Reset Timing (Commercial Temperature)

Item	Symbol	Min	Max	Units
V_{DD}/POR# Rise Time[1]	T_R		200	ms
V_{DD}/POR# Fall Time[2]	T_F		200	ms

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1. V_{DD} Rise Time should be faster than or equal to POR# Rise Time.
2. V_{DD} Fall Time should be slower than or equal to POR# Fall Time.

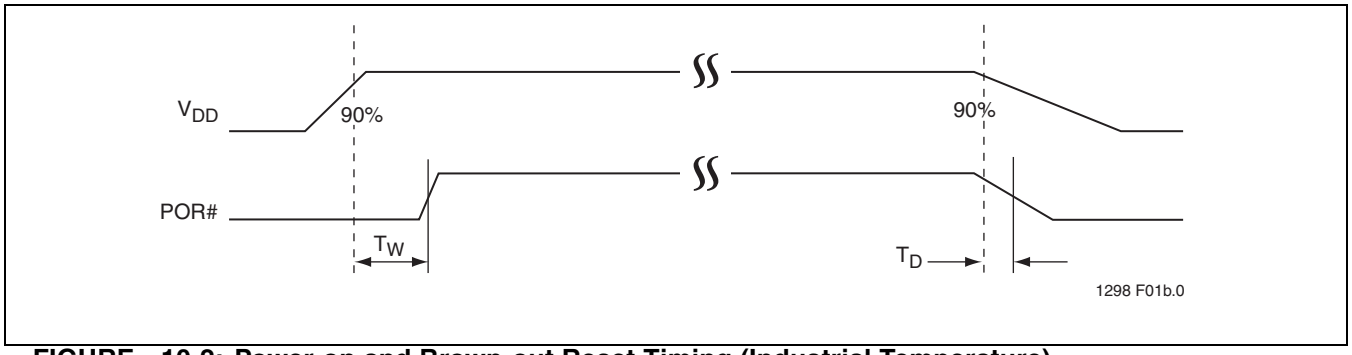

FIGURE 10-2: Power-on and Brown-out Reset Timing (Industrial Temperature)

TABLE 10-2: Power-on and Brown-out Reset Timing (Industrial Temperature)

Item	Symbol	Min	Max	Units
POR Wait Time	T_W	0.1		ms
Brown-out Delay Time	T_D		30	µs

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11.0 I/O TRANSFER FUNCTION

The default operation for the NANDrive is 16-bit. However, if the host issues a Set-Feature command to enable 8-bit mode, the NANDrive permits 8-bit data access.

The following table defines the function of various operations.

TABLE 11-1: I/O Function

Function Code	CS3FX#	CS1FX#	A0-A2	IORD#	IOWR#	D15-D8	D7-D0
Invalid Mode	V_{IL}	V_{IL}	X	X	X	Undefined	Undefined
Standby Mode	V_{IH}	V_{IH}	X	X	X	High Z	High Z
Task File Write	V_{IH}	V_{IL}	1-7H	V_{IH}	V_{IL}	X	Data In
Task File Read	V_{IH}	V_{IL}	1-7H	V_{IL}	V_{IH}	High Z	Data Out
Data Register Write	V_{IH}	V_{IL}	0	V_{IH}	V_{IL}	In[1]	In
Data Register Read	V_{IH}	V_{IL}	0	V_{IL}	V_{IH}	Out[1]	Out
Control Register Write	V_{IL}	V_{IH}	6H	V_{IH}	V_{IL}	X	Control In
Alt Status Read	V_{IL}	V_{IH}	6H	V_{IL}	V_{IH}	High Z	Status Out
Drive Address	V_{IL}	V_{IH}	7H	V_{IL}	V_{IH}	High Z	Data Out

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1. If 8-bit data transfer mode is enabled.
In 8-bit data transfer mode, High Byte is undefined for Data Out. For Data In, X can be V_{IH} or V_{IL}, but no other value.

12.0 SOFTWARE INTERFACE

12.1 NANDrive Drive Register Set Definitions and Protocol

This section defines the drive registers for the NANDrive and the protocol used to address them.

12.1.1 NANDrive Addressing

The I/O decoding for an NANDrive is shown in Table 12-1.

TABLE 12-1: Task File Registers

					Registers	
CS3FX#	**CS1FX#**	**A2**	**A1**	**A0**	**IORD# = 0 (IOWR#=1)**	**IOWR# = 0 (IORD#=1)**
1	0	0	0	0	Data (Read)	Data (Write)
1	0	0	0	1	Error	Feature
1	0	0	1	0	Sector Count	Sector Count
1	0	0	1	1	Sector Number (LBA 7-0)	Sector Number (LBA 7-0)
1	0	1	0	0	Cylinder Low (LBA 15-8)	Cylinder Low (LBA 15-8)
1	0	1	0	1	Cylinder High (LBA 23-16)	Cylinder High (LBA 23-16)
1	0	1	1	0	Drive/Head	Drive/Head
1	0	1	1	1	Status	Command
0	1	1	1	0	Alternate Status	Device Control
0	1	1	1	1	Drive Address	Reserved

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12.1.2 NANDrive Registers

The following section describes the hardware registers used by the host software to issue commands to the NANDrive. These registers are often collectively referred to as the Task File registers. The registers are only selectable through CS3FX#, CS1FX#, and A_2-A_0 signals.

12.1.2.1 Data Register (Read/Write)

This 16-bit register is used to transfer data blocks between the device data buffer and the host. It is also the register through which sector information is transferred on a Format-Track command. Data transfer can be performed in PIO mode.

12.1.2.2 Error Register (Read Only)

This register contains additional information about the source of an error when an error is indicated in bit 0 of the Status register. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0	**Reset Value**
BBK	UNC	0	IDNF	0	ABRT	0	AMNF	**0000 0000b**

Symbol	**Function**
BBK	This bit is set when a Bad Block is detected.
UNC	This bit is set when an Uncorrectable Error is encountered.
IDNF	The requested sector ID is in error or cannot be found.
ABRT	This bit is set if the command has been aborted because of an NANDrive status condition: (Not Ready, Write Fault, etc.) or when an invalid command has been issued. It is required that the host retry any media access command (such as Read-Sectors and Write-Sectors) that ends with an error condition.
AMNF	This bit is set in case of a general error.

12.1.2.3 Feature Register (Write Only)

This register provides information regarding features of the NANDrive that the host can utilize.

12.1.2.4 Sector Count Register

This register contains the numbers of sectors of data requested to be transferred on a Read or Write operation between the host and the NANDrive. If the value in this register is zero, a count of 256 sectors is specified. If the command was successful, this register is zero at command completion. If not successfully completed, the register contains the number of sectors that need to be transferred in order to complete the request.

12.1.2.5 Sector Number (LBA 7-0) Register

This register contains the starting sector number or bits 7-0 of the Logical Block Address (LBA) for any NANDrive data access for the subsequent command.

12.1.2.6 Cylinder Low (LBA 15-8) Register

This register contains the low order 8 bits of the starting cylinder address or bits 15-8 of the Logical Block Address.

12.1.2.7 Cylinder High (LBA 23-16) Register

This register contains the high order bits of the starting cylinder address or bits 23-16 of the Logical Block Address.

12.1.2.8 Drive/Head (LBA 27-24) Register

The Drive/Head register is used to select the drive and head. It is also used to select LBA addressing instead of cylinder/head/sector addressing. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0	**Reset Value**
1	LBA	1	DRV	HS3	HS2	HS1	HS0	**1010 0000b**

Symbol	Function
LBA	LBA is a flag to select either Cylinder/Head/Sector (CHS) or Logical Block Address mode (LBA). When LBA=0, Cylinder/Head/Sector mode is selected. When LBA=1, Logical Block Address is selected. In Logical Block mode, the Logical Block Address is interpreted as follows: LBA7-LBA0: Sector Number register D7-D0. LBA15-LBA8: Cylinder Low register D7-D0. LBA23-LBA16: Cylinder High register D7-D0. LBA27-LBA24: Drive/Head register bits HS3-HS0.
DRV	DRV is the drive number. When DRV=0 (Master), Master is selected. When DRV=1 (Slave), Slave is selected.
HS3	When operating in the Cylinder, Head, Sector mode, this is bit 3 of the head number. It is Bit 27 in the Logical Block Address mode.
HS2	When operating in the Cylinder, Head, Sector mode, this is bit 2 of the head number. It is Bit 26 in the Logical Block Address mode.
HS1	When operating in the Cylinder, Head, Sector mode, this is bit 1 of the head number. It is Bit 25 in the Logical Block Address mode.
HS0	When operating in the Cylinder, Head, Sector mode, this is bit 0 of the head number. It is Bit 24 in the Logical Block Address mode.

12.1.2.9 Status & Alternate Status Registers (Read Only)

These registers return the NANDrive status when read by the host. Reading the Status register does clear a pending interrupt while reading the alternate Status register does not. The meaning of the status bits are described as follows:

D7	D6	D5	D4	D3	D2	D1	D0	Reset Value
BUSY	RDY	DWF	DSC	DRQ	CORR	0	ERR	1000 0000b

Symbol	Function
BUSY	The busy bit is set when the NANDrive has access to the command buffer and registers and the host is locked out from accessing the Command register and buffer. No other bits in this register are valid when this bit is set to a 1.
RDY	RDY indicates whether the device is capable of performing NANDrive operations. This bit is cleared at power up and remains cleared until the NANDrive is ready to accept a command.
DWF	This bit, if set, indicates a write fault has occurred.
DSC	This bit is set when the NANDrive is ready.
DRQ	The Data-Request bit is set when the NANDrive requires that information be transferred either to or from the host through the Data register.
CORR	This bit is set when a correctable data error has been encountered and the data has been corrected. This condition does not terminate a multi-sector Read operation.
ERR	This bit is set when the previous command has ended in some type of error. The bits in the Error register contain additional information describing the error. It is required that the host retry any media access command (such as Read-Sectors and Write-Sectors) that end with an error condition.

12.1.2.10 Device Control Register (Write Only)

This register is used to control the NANDrive interrupt request and to issue a software reset. This register can be written to even if the device is busy. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0	Reset Value
X	X	X	X	1	SW Rst	-IEn	0	0000 1000b

Symbol	Function
SW Rst	This bit is set to 1 in order to force the NANDrive to perform a software Reset operation. The chip remains in reset until this bit is reset to ‘0.’
-IEn	0: The Interrupt Enable bit enables interrupts 1: Interrupts from the NANDrive are disabled This bit is set to 0 at Power-on and Reset.

12.1.2.11 Drive Address Register (Read Only)

This register contains the inverted drive select and head select addresses of the currently selected drive. The bits in this register are as follows:

D7	D6	D5	D4	D3	D2	D1	D0	**Reset Value**
X	-WTG	-HS3	-HS2	-HS1	-HS0	-DS1	-DS0	**x111 1110b**

Symbol	**Function**
-WTG	This bit is 0 when a Write operation is in progress, otherwise, it is 1.
-HS3	This bit is the negation of bit 3 in the Drive/Head register.
-HS2	This bit is the negation of bit 2 in the Drive/Head register.
-HS1	This bit is the negation of bit 1 in the Drive/Head register.
-HS0	This bit is the negation of bit 0 in the Drive/Head register.
-DS1	This bit is 0 when drive 1 is active and selected.
-DS0	This bit is 0 when drive 0 is active and selected.

12.1.2.12 Command Register (Write Only)

This register contains the command code being sent to the drive. Command execution begins immediately after this register is written. The executable commands, the command codes, and the necessary parameters for each command are listed in Table 12-2.

Advance Information

12.2 NANDrive Command Description

This section defines the software requirements and the format of the commands the host sends to the NANDrive. Commands are issued to the NANDrive by loading the required registers in the command block with the supplied parameters, and then writing the command code to the Command register. The manner in which a command is accepted varies. There are three classes (see Table 12-2) of command acceptance, all dependent on the host not issuing commands unless the NANDrive is not busy (BSY=0).

12.2.1 NANDrive Command Set

Table 12-2 summarizes the NANDrive command set with the paragraphs that follow describing the individual commands and the task file for each.

TABLE 12-2: NANDrive Command Set (1 of 2)

Command	Code	FR[1]	SC[2]	SN[3]	CY[4]	DH[5]	LBA[6]
Check-Power-Mode	E5H or 98H	-	-	-	-	D[8]	-
Execute-Drive-Diagnostic	90H	-	-	-	-	D	-
Erase-Sector(s)	C0H	-	Y	Y	Y	Y	Y
Flush-Cache	E7H	-	-	-	-	D	-
Format-Track	50H	-	Y[7]	-	Y	Y[8]	Y
Identify-Drive	ECH	-	-	-	-	D	-
Idle	E3H or 97H	-	Y	-	-	D	-
Idle-Immediate	E1H or 95H	-	-	-	-	D	-
Initialize-Drive-Parameters	91H	-	Y	-	-	Y	-
NOP	00H	-	-	-	-	D	-
Read-Buffer	E4H	-	-	-	-	D	-
Read-DMA	C8H or C9H	-	Y	Y	Y	Y	Y
Read-Long-Sector	22H or 23H	-	-	Y	Y	Y	Y
Read-Multiple	C4H	-	Y	Y	Y	Y	Y
Read-Native-Max-Address	F8H	-	-	-	-	Y	Y
Read-Sector(s)	20H or 21H	-	Y	Y	Y	Y	Y
Read-Verify-Sector(s)	40H or 41H	-	Y	Y	Y	Y	Y
Recalibrate	1XH	-	-	-	-	D	-
Request-Sense	03H	-	-	-	-	D	-
Security-Disable-Password	F6H	-	-	-	-	D	-
Security-Erase-Prepare	F3H	-	-	-	-	D	-
Security-Erase-Unit	F4H	-	-	-	-	D	-
Security-Freeze-Lock	F5H	-	-	-	-	D	-
Security-Set-Password	F1H	-	-	-	-	D	-
Security-Unlock	F2H	-	-	-	-	D	-
Seek	7XH	-	-	Y	Y	Y	Y
Set-Features	EFH	Y	-	-	-	D	-
Set-Max	F9H	-	-	Y	Y	Y	Y
Set-Multiple-Mode	C6H	-	Y	-	-	D	-
Set-Sleep-Mode	E6H or 99H	-	-	-	-	D	-
Set-WP_PD#-Mode	8BH	Y	-	-	-	D	-
Standby	E2H or 96H	-	-	-	-	D	-
Standby-Immediate	E0H or 94H	-	-	-	-	D	-

TABLE 12-2: NANDrive Command Set (Continued) (2 of 2)

Command	Code	FR[1]	SC[2]	SN[3]	CY[4]	DH[5]	LBA[6]
Translate-Sector	87H	-	Y	Y	Y	Y	Y
Write-Buffer	E8H	-	-	-	-	D	-
Write-DMA	CAH or CBH	-	Y	Y	Y	Y	Y
Write-Long-Sector	32H or 33H	-	-	Y	Y	Y	Y
Write-Multiple	C5H	-	Y	Y	Y	Y	Y
Write-Multiple-Without-Erase	CDH	-	Y	Y	Y	Y	Y
Write-Sector(s)	30H or 31H	-	Y	Y	Y	Y	Y
Write-Sector(s)-Without-Erase	38H	-	Y	Y	Y	Y	Y
Write-Verify	3CH	-	Y	Y	Y	Y	Y

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1. FR - Features register
2. SC - Sector Count register
3. SN - Sector Number register
4. CY - Cylinder registers
5. DH - Drive/Head register
6. LBA - Logical Block Address mode supported (see command descriptions for use)
7. Y - The register contains a valid parameter for this command.
8. For the Drive/Head register:Y means both the NANDrive and Head parameters are used;
   D means only the NANDrive parameter is valid and not the Head parameter.

12.2.1.1 Check-Power-Mode - 98H or E5H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	98H or E5H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command checks the power mode. Because the NANDrive can recover from sleep in 200 ns, Idle mode is never enabled. NANDrive sets BSY, sets the Sector Count register to 00H, clears BSY, and generates an interrupt.

12.2.1.2 Erase-Sector(s) - C0H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C0H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

The use of this command is not recommended. This command is effectively a no operation; however, it is supported for backward compatibility.

12.2.1.3 Execute-Drive-Diagnostic - 90H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	90H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command performs the internal diagnostic tests implemented by the NANDrive.

If the Drive bit is ignored and the diagnostic command is executed by both the Master and the Slave with the Master responding with status for both devices.

The diagnostic codes shown in Table 12-3 are returned in the Error register at the end of the command.

TABLE 12-3: Diagnostic Codes

Code	Error Type
01H	No Error Detected
02H	Formatter Device Error
03H	Sector Buffer Error
04H	ECC Circuitry Error
05H	Controlling Microprocessor Error
8XH	Slave Error

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12.2.1.4 Flush-Cache - E7H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E7H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command causes the NANDrive to complete writing data from its cache. The NANDrive then clears BSY and generates an interrupt.

12.2.1.5 Format-Track - 50H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	50H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	X (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command is accepted for host backward compatibility. The NANDrive expects a sector buffer of data from the host to follow the command with the same protocol as the Write-Sector(s) command although the information in the buffer is not used by the NANDrive. The use of this command is not recommended.

12.2.1.6 Identify-Drive - ECH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	ECH							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

The Identify-Drive command enables the host to receive parameter information from the NANDrive. This command has the same protocol as the Read-Sector(s) command. The parameter words in the buffer have the arrangement and meanings defined in Table 12-4. All reserved bits or words are zero. Table 12-4 gives the definition for each field in the Identify-Drive information.

TABLE 12-4: Identify-Drive Information

Word Address	Default Value	Total Bytes	Data Field Type Information
0	044AH	2	General configuration bit
1	bbbbH[1]	2	Default number of cylinders
2	0000H	2	Reserved
3	bbbbH[1]	2	Default number of heads
4	0000H	2	Reserved
5	0000H	2	Reserved
6	bbbbH[1]	2	Default number of sectors per track
7-8	bbbbH[1]	4	Number of sectors per device (Word 7 = MSW, Word 8 = LSW)
9	bbbbH[1]	2	Vendor Unique
10-14	bbbbH[1]	10	User-programmable serial number in ASCII
15-19	bbbbH[1]	10	SST preset, unique ID in ASCII
20	0002H	2	Buffer type
21	0002H	2	Buffer size in 512 Byte increments
22	0004H	2	# of ECC bytes passed on Read/Write-Long-Sector Commands
23-26	bbbbH[1]	8	Firmware revision in ASCII. Big Endian Byte Order in Word
27-46	bbbbH[1]	40	User Definable Model number
47	0001H	2	Maximum number of sectors on Read/Write-Multiple command
48	0000H	2	Reserved
49	0B00H	2	Capabilities
50	0000H	2	Reserved
51	0200H	2	PIO data transfer cycle timing mode
52	0000H	2	Reserved
53	0003H	2	Translation parameters are valid
54	nnnnH[2]	2	Current numbers of cylinders
55	nnnnH[2]	2	Current numbers of heads
56	nnnnH[2]	2	Current sectors per track
57-58	nnnnH[2]	4	Current capacity in sectors (LBAs) (Word 57 = LSW, Word 58 = MSW)
59	0101H	2	Multiple sector setting
60-61	nnnnH[2]	4	Total number of sectors addressable in LBA mode
62	0000H	2	Reserved
63	0n07H[2]	2	DMA data transfer is supported in NANDrive
64	0003H	2	Advanced PIO Transfer mode supported
65	0078H	2	120 ns cycle time support for Multi-word DMA Mode-2
66	0078H	2	120 ns cycle time support for Multi-word DMA Mode-2
67	0078H	2	PIO Mode-4 supported
68	0078H	2	PIO Mode-4 supported
69-79	0000H	22	Reserved
80	007EH	2	ATA/ATAPI major version number
81	0019H	2	ATA/ATAPI minor version number
82	706AH	2	Features/command sets supported
83	410CH	2	Features/command sets supported
84	4000H	2	Features/command sets supported
85-87	xxxxH	6	Features/command sets enabled
88	0000H	2	Reserved
89	xxxxH	2	Time required for security erase unit completion

TABLE 12-4: Identify-Drive Information

Word Address	Default Value	Total Bytes	Data Field Type Information
90	xxxxH	2	Time required for enhanced security erase unit completion
91	xxxxH	2	Current advanced power management value
92-127	0000H	72	Reserved
128	xxxxH	2	Security Status
129-159	0000H	62	Vendor unique bytes
160	xxxxH	2	CFA power mode description
161-255	0000H	190	Reserved

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1. bbbb - default value set by NANDrive.
2. n or nnnn - calculated data based on product configuration

12.2.1.6.1 Word 0: General Configuration

This field informs the host that this is a non-magnetic, hard sectored, removable storage device with a transfer rate greater than 10 MByte/sec and is not MFM encoded.

12.2.1.6.2 Word 1: Default Number of Cylinders

This field contains the number of translated cylinders in the default translation mode. This value will be the same as the number of cylinders.

12.2.1.6.3 Word 3: Default Number of Heads

This field contains the number of translated heads in the default translation mode.

12.2.1.6.4 Word 6: Default Number of Sectors per Track

This field contains the number of sectors per track in the default translation mode.

12.2.1.6.5 Word 7-8: Number of Sectors

This field contains the number of sectors per NANDrive. This double word value is also the first invalid address in LBA translation mode. This field is only required by CF feature set support.

12.2.1.6.6 Word 10-19: Serial Number

An SST preset with unique ID.

12.2.1.6.7 Word 20: Buffer Type

This field defines the buffer capability:

0002H: a dual ported multi-sector buffer capable of simultaneous data transfers to or from the host and the NANDrive.

12.2.1.6.8 Word 21: Buffer Size

This field defines the buffer capacity in 512 Byte increments. SST NANDrive has up to 2 sector data buffer for host interface.

12.2.1.6.9 Word 22: ECC Count

This field defines the number of ECC bytes used on each sector in the Read- and Write-Long-Sector commands.

12.2.1.6.10 Word 23-26: Firmware Revision

This field contains the revision of the firmware for this product.

12.2.1.6.11 Word 27-46: Model Number

This field is reserved for the model number for this product.

12.2.1.6.12 Word 47: Read-/Write-Multiple Sector Count

This field contains the maximum number of sectors that can be read or written per interrupt using the Read-Multiple or Write-Multiple commands.

12.2.1.6.13 Word 49: Capabilities

Bit	Function
13	Standby Timer 0: forces sleep mode when host is inactive.
11	IORDY Support 1: NANDrive supports PIO Mode-4.
9	LBA support 1: NANDrive supports LBA mode addressing.
8	DMA Support 1: DMA mode is supported.

12.2.1.6.14 Word 51: PIO Data Transfer Cycle Timing Mode

This field defines the mode for PIO data transfer. NANDrive supports up to PIO Mode-4.

12.2.1.6.15 Word 53: Translation Parameters Valid

Bit	Function
0	1: words 54-58 are valid and reflect the current number of cylinders, heads and sectors.
1	1: words 64-70 are valid to support PIO Mode-3 and 4.

12.2.1.6.16 Word 54-56: Current Number of Cylinders, Heads, Sectors/Track

These fields contains the current number of user addressable Cylinders, Heads, and Sectors/Track in the current translation mode.

12.2.1.6.17 Word 57-58: Current Capacity

This field contains the product of the current cylinders times heads times sectors.

12.2.1.6.18 Word 59: Multiple Sector Setting

This field contains a validity flag in the Odd Byte and the current number of sectors that can be transferred per interrupt for Read/Write Multiple in the Even Byte. The Odd Byte is always 01H which indicates that the Even Byte is always valid.

The Even Byte value depends on the value set by the Set Multiple command. The Even Byte of this word by default contains a 00H which indicates that Read/Write Multiple commands are not valid.

12.2.1.6.19 Word 60-61: Total Sectors Addressable in LBA Mode

This field contains the number of sectors addressable for the NANDrive in LBA mode only.

12.2.1.6.20 Word 63: Multi-word DMA Transfer Mode

This field identifies the multi-word DMA transfer modes supported by the NANDrive and indicates the mode that is currently selected. Only one DMA mode can be selected at any given time.

Bit	Function
15-11	Reserved
10	Multi-word DMA mode 2 selected 1: Multi-word DMA mode 2 is selected and bits 8 and 9 are cleared to 0 0: Multi-word DMA mode 2 is not selected.
9	Multi-word DMA mode 1 selected 1: Multi-word DMA mode 1 is selected and 8 and 10 should be cleared to 0. 0: Multi-word DMA mode 1 is not selected.
8	Multi-word DMA mode 0 selected 1: Multi-word DMA mode 0 is selected and bits 9 and 10 are cleared to 0. 0: Multi-word DMA mode 0 is not selected.
7-3	Reserved
2	Multi-word DMA mode 2 supported 1: Multi-word DMA mode 2 and below are supported and Bits 0 and 1 are set to 1.
1	Multi-word DMA mode 1 supported 1: Multi-word DMA mode 1 and below are supported.
0	Multi-word DMA mode 0 supported 1: Multi-word DMA mode 0 is supported.

12.2.1.6.21 Word 64: Advanced PIO Data Transfer Mode

Bit	Function
0	1: NANDrive supports PIO Mode-3.
1	1: NANDrive supports PIO Mode-4.

12.2.1.6.22 Word 65: Minimum Multi-word DMA Transfer Cycle Time Per Word

This field defines the minimum Multi-word DMA transfer cycle time per word. This field defines, in nanoseconds, the minimum cycle time that the NANDrive supports when performing Multi-word DMA transfers on a per word basis. SST NANDrive supports up to Multi-word DMA Mode-2, so this field is set to 120ns.

12.2.1.6.23 Word 66: Device Recommended Multi-word DMA Cycle Time

This field defines the NANDrive recommended Multi-word DMA transfer cycle time. This field defines, in nanoseconds, the minimum cycle time per word during a single sector host transfer while performing a multiple sector READ DMA or WRITE DMA command for any location on the media under nominal conditions. If a host runs at a faster cycle rate by operating at a cycle time of less than this value, the NANDrive may negate DMARQ for flow control. The rate at which DMARQ is negated could result in reduced throughput despite the faster cycle rate. Transfer at this rate does not ensure that flow control will not be used, but implies that higher performance may result. SST NANDrive supports up to Multi-word DMA Mode-2, so this field is set to 120 ns.

12.2.1.6.24 Word 67: Minimum PIO Transfer Cycle Time Without Flow Control

The NANDrive's minimum cycle time is 120 ns.

12.2.1.6.25 Word 68: Minimum PIO Transfer Cycle Time With IORDY

The NANDrive's minimum cycle time is 120 ns, e.g., PIO Mode-4.

12.2.1.6.26 Word 80: Major Version Number

If not 0000H or FFFFH, the device claims compliance with the major version(s) as indicated by bits (6:1) being set to one. Since ATA standards maintain downward compatibility, a device may set more than one bit. NANDrive supports ATA-1 to ATA-6.

12.2.1.6.27 Word 81: Minor Version Number

If an implementer claims that the revision of the standard they used to guide their implementation does not need to be reported or if the implementation was based upon a standard prior to the ATA-3 standard, word 81 should be 0000H or FFFFH.

A value of 0019H reported in word 81 indicates ATA/ATAPI-6 T13 1410D revision 3a guided the implementation.

12.2.1.6.28 Words 82-84: Features/command sets supported

Words 82, 83, and 84 indicate the features and command sets supported.

Word 82

Bit	Function
15	0: Obsolete
14	1: NOP command is supported
13	1: Read Buffer command is supported
12	1: Write Buffer command is supported
11	0: Obsolete
10	0: Host Protected Area feature set is not supported
9	0: Device Reset command is not supported
8	0: Service interrupt is not supported
7	0: Release interrupt is not supported
6	1: Look-ahead is supported
5	1: Write cache is supported
4	0: Packet Command feature set is not supported
3	1: Power Management feature set is supported
2	0: Removable Media feature set is not supported
1	1: Security Mode feature set is supported
0	0: SMART feature set is not supported

Word 83

The values in this word should not be depended on by host implementers.

Bit	Function
15	0: Provides indication that the features/command sets supported words are not valid
14	1: Provides indication that the features/command sets supported words are valid
13-9	0: Reserved
8	1: Set-Max security extension supported
7-5	0: Reserved
4	0: Removable Media Status feature set is not supported
3	1: Advanced Power Management feature set is supported
2	1: CFA feature set is supported
1	0: Read DMA Queued and Write DMA Queued commands are not supported
0	0: Download Microcode command is not supported

Word 84

The values in this word should not be depended on by host implementers.

Bit	Function
15	0: Provides indication that the features/command sets supported words are valid
14	1: Provides indication that the features/command sets supported words are valid
13-0	0: Reserved

12.2.1.6.29 Words 85-87: Features/command sets enabled

Words 85, 86, and 87 indicate features/command sets enabled.

The host can enable/disable the features or command set only if they are supported in Words 82-84.

Word 85

Bit	Function
15	0: Obsolete
14	0: NOP command is not enabled 1: NOP command is enabled
13	0: Read Buffer command is not enabled 1: Read Buffer command is enabled
12	0:Write Buffer command is not enabled 1: Write Buffer command is enabled
11	0: Obsolete
10	0: Host Protected Area feature set is not enabled
9	0: Device Reset command is not enabled
8	0: Service interrupt is not enabled
7	0: Release interrupt is not enabled
6	0: Look-ahead is not enabled 1: Look-ahead is enabled
5	0: Write cache is not enabled 1: Write cache is enabled
4	0: Packet Command feature set is not enabled
3	0: Power Management feature set is not enabled 1: Power Management feature set is enabled
2	0: Removable Media feature set is not enabled
1	0: Security Mode feature set has not been enabled via the Security Set Password command 1: Security Mode feature set has been enabled via the Security Set Password command
0	0: SMART feature set is not enabled

Word 86

Bit	Function
15-9	0: Reserved
8	1: Set-Max security extension supported
7-5	0: Reserved
4	0: Removable Media Status feature set is not enabled
3	0: Advanced Power Management feature set is not enabled via the Set Features command 1: Advanced Power Management feature set is enabled via the Set Features command
2	1: CFA feature set is enabled
1	0: Read DMA Queued and Write DMA Queued commands are not enabled
0	0: Download Microcode command is not enabled

Word 87

The values in this word should not be depended on by host implementers.

Bit	Function
15	0: Provides indication that the features/command sets supported words are valid
14	1: Provides indication that the features/command sets supported words are valid
13-0	0: Reserved

12.2.1.6.30 Word 89: Time required for Security erase unit completion

Word 89 specifies the time required for the Security Erase Unit command to complete.

Value	Time
0	Value not specified
1-254	(Value * 2) minutes
255	>508 minutes

12.2.1.6.31 Word 90: Time required for Enhanced security erase unit completion

Word 90 specifies the time required for the Enhanced Security Erase Unit command to complete.

Value	Time
0	Value not specified
1-254	(Value * 2) minutes
255	>508 minutes

12.2.1.6.32 Word 91: Advanced power management level value

Bit	Function
7-0	Current Advanced Power Management level setting

12.2.1.6.33 Word 128: Security Status

Bit	Function
8	Security Level 1: Security mode is enabled and the security level is maximum 0: and security mode is enabled, indicates that the security level is high
5	Enhanced security erase unit feature supported 1: Enhanced security erase unit feature set is supported
4	Expire 1: Security count has expired and Security Unlock and Security Erase Unit are command aborted until a Power-on reset or hard reset
3	Freeze 1: Security is frozen
2	Lock 1: Security is locked
1	Enable/Disable 1: Security is enabled 0: Security is disabled
0	Capability 1: NANDrive supports security mode feature set 0: NANDrive does not support security mode feature set

12.2.1.6.34 Word 160: CFA Power Mode Description

This word indicates the presence and status of a CFA feature set device that supports CFA power mode 1.

Bit	Function
13	Power Level 1 Command Support 1: Power Level 1 commands not supported 0: Power Level 1 commands supported
12	Power Level 1 Command Enable 1: Power Level 1 Commands not enabled 0: Power Level 1 Commands enabled
11-0	This field indicates the maximum average RMS current in mA required during 3.3V or 5V device operation in CFA power mode 1.

12.2.1.7 Idle - 97H or E3H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	97H or E3H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Timer Count (5 msec increments)							
Feature (1)	X							

This command causes the NANDrive to set BSY, enter the Idle mode, clear BSY and generate an interrupt. If the sector count is non-zero, it is interpreted as a timer count with each count being 5 milliseconds and the automatic Power-down mode is enabled. If the sector count is zero, the automatic Power-down mode is also enabled, the timer count is set to 3, with each count being 5 ms. Note that this time base (5 msec) is different from the ATA specification.

12.2.1.8 Idle-Immediate - 95H or E1H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	95H or E1H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command causes the NANDrive to set BSY, enter the Idle mode, clear BSY and generate an interrupt.

12.2.1.9 Initialize-Drive-Parameters - 91H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	91H							
C/D/H (6)	X	0	X	Drive	Max Head (no. of heads-1)			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Number of Sectors							
Feature (1)	X							

This command enables the host to set the number of sectors per track and the number of heads per cylinder. Only the Sector Count and the Drive/Head registers are used by this command.

12.2.1.10 NOP - 00H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	00H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command always fails with the NANDrive returning command aborted.

12.2.1.11 Read-Buffer - E4H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E4H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

The Read-Buffer command enables the host to read the current contents of the NANDrive's sector buffer. This command has the same protocol as the Read-Sector(s) command

12.2.1.12 Read-DMA - C8H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C8H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command executes in a similar manner to the Read-Sector(s) command except for the following:
- the host initializes the DMA channel prior to issuing the command;
- data transfers are qualified by DMARQ and are performed by the DMA channel;
- the NANDrive issues only one interrupt per command to indicate that data transfer has terminated and status is available.

During the DMA transfer phase of a Read-DMA command, the NANDrive will provide the status of the BSY bit or the DRQ bit until the command is completed.

12.2.1.13 Read-Multiple - C4H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C4H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Note: The current revision of the NANDrive can support up to a block count of 1 as indicated in the Identify-Drive Command information.

The Read-Multiple command is similar to the Read-Sector(s) command. Interrupts are not generated on every sector, but on the transfer of a block which contains the number of sectors defined by a Set Multiple command.

Command execution is identical to the Read-Sectors operation except that the number of sectors defined by a Set Multiple command are transferred without intervening interrupts. DRQ qualification of the transfer is required only at the start of the data block, not on each sector.

The block count of sectors to be transferred without intervening interrupts is programmed by the Set-Multiple-Mode command, which must be executed prior to the Read-Multiple command. When the Read-Multiple command is issued, the Sector Count register contains the number of sectors (not the number of blocks or the block count) requested. If the number of requested sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where

n = remainder (sector count/block count).

If the Read-Multiple command is attempted before the Set-Multiple-Mode command has been executed or when Read-Multiple commands are disabled, the Read-Multiple operation is rejected with an

Aborted Command error. Disk errors encountered during Read-Multiple commands are posted at the beginning of the block or partial block transfer, but DRQ is still set and the data transfer will take place as it normally would, including transfer of corrupted data, if any.

Interrupts are generated when DRQ is set at the beginning of each block or partial block. The error reporting is the same as that on a Read-Sector(s) command. This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number register.

At command completion, the Command Block registers contain the cylinder, head and sector number of the last sector read.

If an error occurs, the read terminates at the sector where the error occurred. The Command Block registers contain the cylinder, head and sector number of the sector where the error occurred. The flawed data is pending in the sector buffer.

Subsequent blocks or partial blocks are transferred only if the error was a correctable data error. All other errors cause the command to stop after transfer of the block which contained the error.

12.2.1.14 Read-Long-Sector - 22H or 23H

Bit ->	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Command (7)	22H or 23H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	X							
Feature (1)	X							

The Read-Long-Sector command performs similarly to the Read-Sector(s) command except that it returns 516 Bytes of data instead of 512 Bytes. During a Read-Long-Sector command, the NANDrive does not check the ECC bytes to determine if there has been a data error. Only single-sector Read-Long-Sector operations are supported. The transfer consists of 512 Bytes of data transferred in Word-Mode followed by 4 Bytes of ECC data transferred in Byte-Mode. This command has the same protocol as the Read-Sector(s) command. Use of this command is not recommended.

12.2.1.15 Read-Native-Max-Address - F8H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	F8H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command returns the native maximum address. The native maximum address is the highest address accepted by the device in the factory default condition. The native maximum address is the maximum address that is valid when using the Set-Max-Address command.

The Read-Native-Max-Address command output will take the following format:

Bit ->	7	6	5	4	3	2	1	0
C/D/H	X			Drive	Native max address (LBA 27:24)			
Cyl High	Native max address (LBA 23-16)							
Cyl Low	Native max address (LBA 15-8)							
Sec Num	Native max address (LBA 7-0)							
Sec Cnt	X							

C/D/H — Maximum native LBA bits (27:24) for native max address on the device. Drive indicates the selected device.

Cyl High — Maximum native LBA bits (23:16) for native max address on the device.

Cyl Low — Maximum native LBA bits (15:8) for native max address on the device.

Sec Num — Maximum native LBA bits (7:0) for native max address on the device.

12.2.1.16 Read-Sector(s) - 20H or 21H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	20H or 21H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number register. When this command is issued and after each sector of data (except the last one) has been read by the host, the NANDrive sets BSY, puts the sector of data in the buffer, sets DRQ, clears BSY, and generates an interrupt. The host then reads the 512 Bytes of data from the buffer.

At command completion, the Command Block registers contain the cylinder, head and sector number of the last sector read. If an error occurs, the read terminates at the sector where the error occurred. The Command Block registers contain the cylinder, head, and sector number of the sector where the error occurred. The flawed data is pending in the sector buffer.

12.2.1.17 Read-Verify-Sector(s) - 40H or 41H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	40H or 41H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command is identical to the Read-Sectors command, except that DRQ is never set and no data is transferred to the host. When the command is accepted, the NANDrive sets BSY.

When the requested sectors have been verified, the NANDrive clears BSY and generates an interrupt. Upon command completion, the Command Block registers contain the cylinder, head, and sector number of the last sector verified.

If an error occurs, the verify terminates at the sector where the error occurs. The Command Block registers contain the cylinder, head and sector number of the sector where the error occurred. The Sector Count register contains the number of sectors not yet verified.

12.2.1.18 Recalibrate - 1XH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	1XH							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command is effectively a no operation and is provided for compatibility purposes.

12.2.1.19 Request-Sense - 03H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	03H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command requests extended error information for the previous command. Table 12-5 defines the valid extended error codes for the NANDrive. The extended error code is returned to the host in the Error register.

TABLE 12-5: Extended Error Codes

Extended Error Code	Description
00H	No Error Detected
01H	Self Test OK (No Error)
09H	Miscellaneous Error
20H	Invalid Command
21H	Invalid Address (Requested Head or Sector Invalid)
2FH	Address Overflow (Address Too Large)
35H, 36H	Supply or generated Voltage Out of Tolerance
11H	Uncorrectable ECC Error
18H	Corrected ECC Error
05H, 30-34H, 37H, 3EH	Self Test or Diagnostic Failed
10H, 14H	ID Not Found
3AH	Spare Sectors Exhausted
1FH	Data Transfer Error / Aborted Command
0CH, 38H, 3BH, 3CH, 3FH	Corrupted Media Format
03H	Write / Erase Failed
22H	Power Level 1 Disabled

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12.2.1.20 Security-Disable-Password - F6H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	F6H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command requests a transfer of a single sector of data from the host. Table 12-6 defines the content of this sector of information. If the password selected by Word 0 matches the password previously saved by the device, the device disables the lock mode. This command does not change the Master password that may be reactivated later by setting a User password.

TABLE 12-6: Security Password Data Content

Word	Content
0	Control Word Bit 0: Identifier 0: Compare User Password 1: Compare Master Password Bit 1-15: Reserved
1-16	Password (32 Bytes)
17-256	Reserved

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12.2.1.21 Security-Erase-Prepare - F3H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	F3H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command is issued immediately before the Security-Erase-Unit command to enable device erasing and unlocking. This command prevents accidental erasure of the data in the flash media.

12.2.1.22 Security-Erase-Unit - F4H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	F4H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command requests transfer of a single sector of data from the host. Table 12-6 defines the content of this sector of information. If the password does not match the password previously saved by the NANDrive, the NANDrive rejects the command with command aborted. The Security-Erase-Prepare command should be completed immediately prior to the Security-Erase-Unit command. If the NANDrive receives a Security-Erase-Unit command without an immediately prior Security-Erase-Prepare command, the NANDrive aborts the Security-Erase-Unit command.

12.2.1.23 Security-Freeze-Lock - F5H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	F5H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

The Security-Freeze-Lock command sets the NANDrive to Frozen mode. After command completion, any other commands that update the NANDrive Lock mode are rejected. Frozen mode is disabled by power off or hardware reset. If Security-Freeze-Lock is issued when the NANDrive is in Frozen mode, the command executes and the NANDrive remains in Frozen mode. After command completion, the sector count register should be set to 0. Commands disabled by Security-Freeze-Lock are:

- Security-Set-Password
- Security-Unlock
- Security-Disable-Password
- Security-Erase-Unit

If security mode feature set is not supported, this command will be handled as an invalid command.

12.2.1.24 Security-Set-Password - F1H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	F1H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command requests a transfer of a single sector of data from the host. Table 12-7 defines the content of the sector of information. The data transferred controls the function of this command.

TABLE 12-7: Security Password Data Content

Word	Content
0	Control Word Bit 0: Identifier 0: Compare User Password 1: Compare Master Password Bit 1-15: Reserved
1-16	Password (32 Bytes)
17-256	Reserved

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Table 12-8 defines the interaction of the identifier and security level bits.

TABLE 12-8: Identifier and Security Level Bit Interaction

Identifier	Level	Command result
User	High	The password supplied with the command is saved as the new User password. The lock mode will be enabled from the next Power-on or hardware reset. The NANDrive will then be unlocked by either the User password or the previously set Master password.
User	Maximum	The password supplied with the command is saved as the new user password. The Lock mode will be enabled from the next Power-on reset or hardware reset. The NANDrive will then be unlocked by only the User password. The Master password previously set is still stored in the NANDrive will not be used to unlock the NANDrive.
Master	High or Maximum	This combination sets a Master password but does not enable or disable the Lock mode. The security level is not changed.

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12.2.1.25 Security-Unlock- F2H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	F2H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command requests transfer of a single sector of data from the host. Table 12-6 defines the content of this sector of information. If the identifier bit is set to Master and the device is in high security level, then the password supplied is compared with the stored Master password. If the device is in the maximum security level, then the unlock command will be rejected. If the identifier bit is set to user, then the device compares the supplied password with the stored User password. If the password compare fails, the device returns “command aborted” to the host and decrements the unlock counter. This counter is initially set to five and is decremented for each password mismatch when Security-Unlock is issued and the device is locked. Once this counter reaches zero, the Security-Unlock and Security-Erase-Unit commands are command aborted until after a Power-on reset or a hardware reset is received. Security-Unlock commands issued when the device is unlocked have no effect on the unlock counter.

12.2.1.26 Seek - 7XH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	7XH							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	X (LBA 7-0)							
Sec Cnt (2)	X							
Feature (1)	X							

This command is effectively a no operation, although it does perform a range check of cylinder and head or LBA address and returns an error if the address is out of range.

12.2.1.27 Set-Features - EFH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	EFH							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Config							
Feature (1)	Feature							

This command is used by the host to establish or select certain features. Table 12-9 defines all features that are supported.

TABLE 12-9: Features Supported

Feature	Operation
01H	Enable 8-bit data transfers.
02H	Enable Write cache
03H	Set transfer mode based on value in Sector Count register. Table 12-11 defines the values.
05H	Enable Advanced Power Management
09H	Enable Extended Power Operations
0AH	Enable Power Level 1 commands
55H	Disable Read Look Ahead.
66H	Disable Power-on Reset (POR) establishment of defaults at software reset.
69H	NOP - Accepted for backward compatibility.
81H	Disable 8-bit data transfer.
82H	Disable Write Cache
85H	Disable Advanced Power Management
89H	Disable Extended Power operations
8AH	Disable Power Level 1 commands
96H	NOP - Accepted for backward compatibility.
97H	Accepted for backward compatibility. Use of this Feature is not recommended.
9AH	Set the host current source capability Allows trade-off between current drawn and Read/Write speed
BBH	4 Bytes of data apply on Read/Write-Long-Sector commands.
AAH	Enable Read-Look-Ahead
CCH	Enable Power-on Reset (POR) establishment of defaults at software reset.

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Features 01H and 81H are used to enable and clear 8-bit data transfer mode. If the 01H feature command is issued all data transfers will occur on the low order D_7-D_0 data bus and the IOCS16# signal will not be asserted for data register accesses.

Features 02H and 82H allow the host to enable or disable write cache in the NANDrives that implement write cache. When the subcommand Disable-Write-Cache is issued, the NANDrive should initiate the sequence to flush cache to non-volatile memory before command completion.

Feature 03H allows the host to select the transfer mode by specifying a value in the Sector Count register. The upper 5 bits define the type of transfer and the low order 3 bits encode the mode value. One PIO mode is selected at all times. The host may change the selected modes by the Set-Features command.

Feature 05H allows the host to enable advanced power management. To enable advanced power management, the host writes the Sector Count register with the desired advanced power management level and then executes a Set-Features command with subcommand code 05H. The power management level is a scale from the lowest power consumption setting of 01H to the maximum performance level of FEH. Table 12-10 shows these values.

TABLE 12-10: Advanced Power Management Levels

Level	Sector Count Value
Maximum performance	FEH
Intermediate power management levels without standby	81H-FDH
Minimum power consumption without standby	80H
Intermediate power management levels with standby	02H-7FH
Minimum power consumption with standby	01H
Reserved	FFH
Reserved	00H

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Device performance may increase with increasing power management levels. Device power consumption may increase with increasing power management levels. The power management levels may contain discrete bands. For example, a NANDrive may implement one power management method from 80H to A0H and a higher performance, higher power consumption method from level A1H to FEH.

Feature 85H disables Advanced Power Management. Subcommand 85H may not be implemented on all devices that implement Set Features subcommand 05H.

Features 0AH and 8AH are used to enable and disable Power Level 1 commands. Feature 0AH is the default feature for the NANDrive with extended power.

Features 55H and BBH are the default features for the NANDrive; thus, the host does not have to issue this command with these features unless it is necessary for compatibility reasons.

Feature code 9AH enables the host to configure the device to best meet the host system's power requirements. The host sets a value in the Sector Count register that is equal to one-fourth of the desired maximum average current (in mA) that the device should consume. For example, if the Sector Count register is set to 6, the device would be configured to provide the best possible performance without exceeding 24 mA. Upon completion of the command, the device responds to the host with the range of values supported by the device. The minimum value is set in the Cylinder Low register, and the maximum value is set in the Cylinder High register. The default value, after a power on reset, is to operate at the highest performance and therefore the highest current mode.

The device will accept values outside this programmable range, but will operate either at the lowest power or highest performance as appropriate.

Features 66H and CCH can be used to enable and disable whether the Power-on Reset (POR) Defaults will be set when a software reset occurs.

TABLE 12-11: Transfer Mode Values

Mode	Bits [7:3]	Bits [2:0]
PIO default mode	00000b	000b
PIO default mode, disable IORDY	00000b	001b
PIO flow control transfer mode	00001b	mode[1]
Multi-word DMA mode	00100b	mode[1]
Reserved	Other	N/A

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1. Mode = transfer mode number, all other values are not valid

12.2.1.28 Set-Max - F9H

Individual Set-Max commands are identified by the value placed in the Features register. Table 12-12 shows these Features register values.

TABLE 12-12: Set-Max Features register values

Value	Command
00H	Obsolete
01H	Set-Max-Set-Password
02H	Set-Max-Lock
03H	Set-Max-Unlock
04H	Set-Max-Freeze-Lock
05H-FFH	Reserved

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12.2.1.28.1 Set-Max-Address - F9H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	F9H							
C/D/H (6)	1	LBA	1	Drive	Native max address head number or Set-Max LBA			
Cyl High (5)	Set-Max cylinder high or LBA							
Cyl Low (4)	Set-Max cylinder low or LBA							
Sec Num (3)	Native max address sector number or Set-Max LBA							
Sec Cnt (2)	X							VV
Feature (1)	X							

The Set-Max-Address command must be immediately preceded by a successful execution of a Read-Native-Max-Address command. Otherwise the Set-Max-Address command will be interpreted as another Set-Max command or aborted as an invalid command.

C/D/H

LBA — 1: The maximum address value is an LBA value.
0: The maximum address value is a CHS value.

Drive — The selected device.

Bits (3:0) — The native max address head number (Identify-Device word 3 minus one) or LBA bits (27:24) value to be set.

Cyl High — Contains the maximum cylinder high or LBA bits (23:16) value to be set

Cyl Low — Contains the maximum cylinder low or LBA bits (15:8) value to be set

Sec Num — Contains the native max address sector number (Identify-Device word 6) or LBA bits (7:0) value to be set

Sec Cnt

VV — Value Volatile
1: The device preserves the maximum values over Power-on or hardware reset.
0: The device reverts to the most recent non-volatile maximum address value setting over Power-on or hardware reset.

After successful command completion, all Read and Write access attempts to addresses greater than specified by the successful Set-Max-Address command is rejected with an IDNF error. Identify-Device response words 1, 54, 57, 58, 60, and 61 reflect the maximum address set with this command.

Hosts should not issue more than one non-volatile Set-Max-Address command after a Power-on or hardware reset. Devices should report an IDNF error upon receiving a second non-volatile Set-Max-Address command after a Power-on or hardware reset.

The contents of Identify-Device words and the max address will not be changed if a Set-Max-Address command fails.

After a successful Set-Max-Address command using a new maximum cylinder number value the content of all Identify-Device words must comply with the following:

1. The content of words 3, 6, 55, and 56 are unchanged
2. The content of word 1 will equal (the new Set-Max cylinder number + 1) or 16,383, whichever is less
3. The content of words (61:60) equals [(the new content of word 1 as determined by the successful Set-Max-Address command) * (the content of word 3) * (the content of word 6)]

4. If the content of words (61:60) as determined by a successful Set-Max-Address command is less than 16,514,064, then the content of word 54 should be equal to [(the content of words (61:60)) ÷ ((the content of Identify-Device word 55) * (the content of word 56)] or 65,535, whichever is less.
5. If the content of word (61:60), as determined by a successful Set-Max-Address command, is greater than 16,514,064, then word 54 should equal the whole number result of [[(16,514,064) ÷ [(the content of word 55) * (the content of word 56)]] or 65,535 whichever is less). The content of words (58:57) should be equal to [(the new content of word 54 as determined by the successful Set-Max-Address command) * (the content of word 55) * (the content of word 56)].

After a successful Set-Max-Address command using a new maximum LBA address the content of all Identify-Device words must comply with the following:

- The content of words (61:60) should equal the new Maximum LBA address + 1.
- If the content of words (61:60) is greater than 16,514,064 and if the device does not support CHS addressing, then the content of words 1, 3, 6, 54, 55, 56, and (58:57) should equal zero.

If the device supports CHS addressing:

- The content of words 3, 6, 55, and 56 are unchanged.
- If the new content of words (61:60) is less than 16,514,064, then the content of word 1 should equal [(the new content of words (61:60)) ÷ [(the content of word 3) * (the content of word 6)]] or 65,535, whichever is less.
- If the new content of words (61:60) is greater than or equal to 16,514,064, then the content of word 1 should be equal to 16,383.
- If the new content of words (61:60) is less than 16,514,064, then the content of word 54 should equal [(the new content of words (61:60)) ÷ [(the content of word 55) * (the content of word 56)]].
- If the new content of words (61:60) is greater than or equal to 16,514,064, then the content of word 54 should equal 16,383.
- Words (58:57) should equal [(the content of word 54) * (the content of word 55) * (the content of word 56).

12.2.1.28.2 Set-Max-Set-Password

F9H with the content of the Features register equal to 01H.

Bit ->	7	6	5	4	3	2	1	0
Command (7)	F9H							
C/D/H (6)	X			Drive	N/A			
Cyl High (5)	N/A							
Cyl Low (4)	N/A							
Sec Num (3)	N/A							
Sec Cnt (2)	N/A							
Feature (1)	01H							

This command requests a transfer of a single sector of data from the host. Table 12-1 defines the content of this sector of information. The password is retained by the device until the next power cycle. When the device accepts this command, the device is in Set_Max_Locked state.

If this command is immediately preceded by a Read-Native-Max-Address command, it will be interpreted as a Set-Max-Address command.

TABLE 12-13: Set-Max-Set-Password Data Content

Word	Content
0	Reserved
1-16	Password (32 Bytes)
17-255	Reserved

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12.2.1.28.3 Set-Max-Lock

F9H with the content of the Features register equal to 02H.

Bit ->	7	6	5	4	3	2	1	0
Command (7)	F9H							
C/D/H (6)	X			Drive	N/A			
Cyl High (5)	N/A							
Cyl Low (4)	N/A							
Sec Num (3)	N/A							
Sec Cnt (2)	N/A							
Feature (1)	02H							

The Set-Max-Lock command sets the device into Set_Max_Locked state. After this command is completed, any other Set-Max commands except Set-Max-Unlock and Set-Max-Freeze-Lock are rejected. The device remains in this state until a power cycle or the acceptance of a Set-Max-Unlock or Set-Max-Freeze-Lock command.

If this command is immediately preceded by a Read-Native-Max-Address command, it will be interpreted as a Set-Max-Address command.

12.2.1.28.4 Set-Max-Unlock

F9H with the content of the Features register equal to 03H.

Bit ->	7	6	5	4	3	2	1	0
Command (7)	F9H							
C/D/H (6)	X			Drive	N/A			
Cyl High (5)	N/A							
Cyl Low (4)	N/A							
Sec Num (3)	N/A							
Sec Cnt (2)	N/A							
Feature (1)	03H							

This command requests a transfer of a single sector of data from the host. Table 12-13 defines the content of this sector of information.

The password supplied in the sector of data transferred will be compared with the stored Set-Max password.

If the password compare fails, then the device returns command aborted and decrements the unlock counter. On the acceptance of the Set-Max-Lock command, this counter is set to a value of five and is decremented for each password mismatch when Set-Max-Unlock is issued and the device is locked. When this counter reaches zero, then the Set-Max-Unlock command returns “command aborted” until a power cycle.

If the password compare matches, then the device transitions to the Set_Max_Unlocked state and all Set-Max commands will be accepted.

If this command is immediately preceded by a Read-Native-Max-Address command, it will be interpreted as a Set-Max-Address command.

12.2.1.28.5 Set-Max-Freeze-Lock

F9H with the content of the Features register equal to 04H.

Bit ->	7	6	5	4	3	2	1	0
Command (7)	F9H							
C/D/H (6)	X			Drive	N/A			
Cyl High (5)	N/A							
Cyl Low (4)	N/A							
Sec Num (3)	N/A							
Sec Cnt (2)	N/A							
Feature (1)	04H							

The Set-Max-Freeze-Lock command sets the device to Set_Max_Frozen state. After command completion any subsequent Set-Max commands are rejected.

Commands disabled by Set-Max-Freeze-Lock are:

- Set-Max-Address
- Set-Max-Set-Password
- Set-Max-Lock
- Set-Max-Unlock

If this command is immediately preceded by a Read-Native-Max-Address command, it will be interpreted as a Set-Max-Address command.

12.2.1.29 Set-Multiple-Mode - C6H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C6H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command enables the NANDrive to perform Read and Write-Multiple operations and establishes the block count for these commands. The Sector Count register is loaded with the number of sectors per block. Upon receipt of the command, the NANDrive sets BSY to 1 and checks the Sector Count register.

If the Sector Count register contains a valid value (see Section 12.2.1.6.12 for details) and the block count is supported, the value is loaded for all subsequent Read-Multiple and Write-Multiple commands and execution of those commands is enabled. If a block count is not supported, an Aborted Command error is posted, and Read-Multiple and Write-Multiple commands are disabled. If the Sector Count register contains 0 when the command is issued, Read and Write-Multiple commands are disabled. At power on, or after a hardware or (unless disabled by a Set Feature command) software reset, the default mode is Read and Write-Multiple disabled.

12.2.1.30 Set-Sleep-Mode - 99H or E6H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	99H or E6H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command causes the NANDrive to set BSY, enter the Sleep mode, clear BSY and generate an interrupt. Recovery from sleep mode is accomplished by simply issuing another command (a reset is permitted but not required). Sleep mode is also entered when internal timers expire so the host does not need to issue this command except when it wishes to enter Sleep mode immediately. The default value for the timer is 15 milliseconds.

12.2.1.31 Set-WP_PD#-Mode - 8BH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	8BH							
C/D/H (6)	X			Drive	X			
Cyl High (5)	6EH							
Cyl Low (4)	44H							
Sec Num (3)	72H							
Sec Cnt (2)	50H							
Feature (1)	55H or AAH							

This command configures the WP_PD# pin for either the Write Protect mode or the Power-down mode. When the host sends this command to the device with the value AAH in the feature register, the WP_PD# pin is configured for the Write Protect mode described in Section 7.1. The Write Protect mode is the factory default setting. When the host sends this command to the device with the value 55H in the feature register, WP_PD# is configured for the Power-down mode.

All values in the C/D/H register, the Cylinder Low register, the Cylinder High register, the Sector Number register, the Sector Count register, and the Feature register need to match the values shown above, otherwise, the command will be treated as an invalid command.

Once the mode is set with this command, the device will stay in the configured mode until the next time this command is issued. Power-off or reset will not change the configured mode.

12.2.1.32 Standby - 96H or E2H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	96H or E2H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command causes the NANDrive to set BSY, enter the Sleep mode (which corresponds to the ATA “Standby” mode), clear BSY and return the interrupt immediately. Recovery from sleep mode is accomplished by simply issuing another command (a reset is not required).

12.2.1.33 Standby-Immediate - 94H or E0H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	94H or E0H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command causes the NANDrive to set BSY, enter the Sleep mode (which corresponds to the ATA "Standby" mode), clear BSY and return the interrupt immediately. Recovery from sleep mode is accomplished by simply issuing another command (a reset is not required).

12.2.1.34 Translate-Sector - 87H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	87H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	X							
Feature (1)	X							

This command allows the host a method of determining the exact number of times a user sector has been erased and programmed. The NANDrive responds with a 512 Byte buffer of information containing the desired cylinder, head, and sector, including its logical address, and the Hot Count, if available, for that sector. Table 12-14 represents the information in the buffer. Please note that this command is unique to the NANDrive.

TABLE 12-14: Translate Sector Information

Address	Information
00H-01H	Cylinder MSB (00), Cylinder LSB (01)
02H	Head
03H	Sector
04H-06H	LBA MSB (04) - LSB (06)
07H-12H	Reserved
13H	Erased Flag (FFh) = Erased; 00h = Not Erased
14H-17H	Reserved
18H-1AH	Hot Count MSB (18) - LSB (1A)[1]
1BH-1FFH	Reserved

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1. A value of 0 indicates Hot Count is not supported.

12.2.1.35 Write-Buffer - E8H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E8H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

The Write-Buffer command enables the host to overwrite contents of the NANDrive's sector buffer with any data pattern desired. This command has the same protocol as the Write-Sector(s) command and transfers 512 Bytes.

12.2.1.36 Write-DMA - CAH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	CAH							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command executes in a similar manner to Write-Sector(s) except for the following:
- the host initializes the DMA channel prior to issuing the command;
- data transfers are qualified by DMARQ and are performed by the DMA channel;
- the NANDrive issues only one interrupt per command to indicate that data transfer has terminated and status is available. During the execution of a WRITE DMA command, the NANDrive will provide status of the BSY bit or the DRQ bit until the command is completed.

12.2.1.37 Write-Long-Sector - 32H or 33H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	32H or 33H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	X							
Feature (1)	X							

This command is similar to the Write-Sector(s) command except that it writes 516 Bytes instead of 512 Bytes. Only single sector Write-Long-Sector operations are supported. The transfer consists of 512 Bytes of data transferred in Word-Mode followed by 4 Bytes of ECC transferred in Byte-Mode. Because of the unique nature of the solid-state NANDrive, the 4 Bytes of ECC transferred by the host may be

used by the NANDrive. The NANDrive may discard these 4 Bytes and write the sector with valid ECC data. This command has the same protocol as the Write-Sector(s) command. Use of this command is not recommended.

12.2.1.38 Write-Multiple - C5H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C5H							
C/D/H (6)	1	LBA	1	Drive	Head			
Cyl High (5)	Cylinder High							
Cyl Low (4)	Cylinder Low							
Sec Num (3)	Sector Number							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Note: The current revision of the NANDrive can support up to a block count of 1 as indicated in the Identify-Drive Command information.

This command is similar to the Write-Sectors command. The NANDrive sets BSY within 400 ns of accepting the command. Interrupts are not presented on each sector but on the transfer of a block which contains the number of sectors defined by Set Multiple. Command execution is identical to the Write-Sectors operation except that the number of sectors defined by the Set Multiple command is transferred without intervening interrupts.

DRQ qualification of the transfer is required only at the start of the data block, not on each sector. The block count of sectors to be transferred without intervening interrupts is programmed by the Set-Multiple-Mode command, which must be executed prior to the Write-Multiple command.

When the Write-Multiple command is issued, the Sector Count register contains the number of sectors (not the number of blocks or the block count) requested. If the number of requested sectors is not evenly divisible by the sector/block, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where:

n = remainder (sector count/block).

If the Write-Multiple command is attempted before the Set-Multiple-Mode command has been executed or when Write-Multiple commands are disabled, the Write-Multiple operation will be rejected with an aborted command error.

Errors encountered during Write-Multiple commands are posted after the attempted writes of the block or partial block transferred. The Write command ends with the sector in error, even if it is in the middle of a block. Subsequent blocks are not transferred in the event of an error. Interrupts are generated when DRQ is set at the beginning of each block or partial block.

The Command Block registers contain the cylinder, head and sector number of the sector where the error occurred and the Sector Count register contains the residual number of sectors that need to be transferred for successful completion of the command e.g. each block has 4 sectors, a request for 8 sectors is issued and an error occurs on the third sector. The Sector Count register contains 6 and the address is that of the third sector.

12.2.1.39 Write-Multiple-Without-Erase - CDH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	CDH							
C/D/H (6)	1	LBA	1	Drive	Head			
Cyl High (5)	Cylinder High							
Cyl Low (4)	Cylinder Low							
Sec Num (3)	Sector Number							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Use of this command is not recommended, but it is supported as Write-Multiple command for backward compatibility.

12.2.1.40 Write-Sector(s) - 30H or 31H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	30H or 31H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command writes from 1 to 256 sectors as specified in the Sector Count register. A sector count of zero requests 256 sectors. The transfer begins at the sector specified in the Sector Number register. When this command is accepted, the NANDrive sets BSY, then sets DRQ and clears BSY, then waits for the host to fill the sector buffer with the data to be written. No interrupt is generated to start the first host transfer operation. No data should be transferred by the host until BSY has been cleared by the host.

For multiple sectors, after the first sector of data is in the buffer, BSY will be set and DRQ will be cleared. After the next buffer is ready for data, BSY is cleared, DRQ is set and an interrupt is generated. When the final sector of data is transferred, BSY is set and DRQ is cleared. It will remain in this state until the command is completed at which time BSY is cleared and an interrupt is generated.

If an error occurs during a write of more than one sector, writing terminates at the sector where the error occurs. The Command Block registers contain the cylinder, head and sector number of the sector where the error occurred. The host may then read the command block to determine what error has occurred, and on which sector.

12.2.1.41 Write-Sector(s)-Without-Erase - 38H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	38H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Use of this command is not recommended, but it is supported as Write-Sector(s) command for backward compatibility.

12.2.1.42 Write-Verify - 3CH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	3CH							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command is similar to the Write-Sector(s) command, except each sector is verified immediately after being written. This command has the same protocol as the Write-Sector(s) command.

12.2.2 Error Posting

The following table summarizes the valid status and error values for the NANDrive command set.

TABLE 12-15: Error and Status Register[1] (1 of 2)

	Error Register					Status Register				
Command	**BBK**	**UNC**	**IDNF**	**ABRT**	**AMNF**	**RDY**	**DWF**	**DSC**	**CORR**	**ERR**
Check-Power-Mode				V		V	V	V		V
Execute-Drive-Diagnostic[2]						V		V		V
Erase-Sector(s)	V		V	V	V	V	V	V		V
Flush-Cache				V		V	V	V		V
Format-Track			V	V	V	V	V	V		V
Identify-Drive				V		V	V	V		V
Idle				V		V	V	V		V
Idle-Immediate				V		V	V	V		V
Initialize-Drive-Parameters						V		V		V
NOP				V		V	V			V
Read-Buffer				V		V	V	V		V
Read-DMA	V	V	V	V	V	V	V	V	V	V
Read-Long-Sector	V		V	V	V	V	V	V		V
Read-Multiple	V	V	V	V	V	V	V	V	V	V
Read-Native-Max-Address						V	V			V
Read-Sector(s)	V	V	V	V	V	V	V	V	V	V
Read-Verify-Sector(s)	V	V	V	V	V	V	V	V	V	V
Recalibrate				V		V	V	V		V
Request-Sense				V		V		V		V
Security-Disable-Password				V		V	V	V		V
Security-Erase-Prepare				V		V	V	V		V
Security-Erase-Unit				V		V	V	V		V
Security-Freeze-Lock				V		V	V	V		V
Security-Set-Password				V		V	V	V		V
Security-Unlock				V		V	V	V		V
Seek			V	V		V	V	V		V
Set-Features				V		V	V	V		V
Set-Max			V	V		V				V
Set-Multiple-Mode				V		V	V	V		V
Set-Sleep-Mode				V		V	V	V		V
Set-WP_PD#-Mode				V		V		V		V
Standby				V		V	V	V		V
Standby-Immediate				V		V	V	V		V
Translate-Sector	V		V	V	V	V	V	V		V
Write-Buffer				V		V	V	V		V
Write-DMA	V		V	V	V	V	V	V		V
Write-Long-Sector	V		V	V	V	V	V	V		V
Write-Multiple	V		V	V	V	V	V	V		V
Write-Multiple-Without-Erase	V		V	V	V	V	V	V		V

TABLE 12-15: Error and Status Register[1] (Continued) (2 of 2)

	Error Register					Status Register				
Command	**BBK**	**UNC**	**IDNF**	**ABRT**	**AMNF**	**RDY**	**DWF**	**DSC**	**CORR**	**ERR**
Write-Sector(s)	V		V	V	V	V	V	V		V
Write-Sector(s)-Without-Erase	V		V	V	V	V	V	V		V
Write-Verify	V		V	V	V	V	V	V		V
Invalid-Command-Code				V		V	V	V		V

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1. The host is required to reissue any media access command (such as Read-Sector and Write Sector) that ends with an error condition.
2. See Table 12-3
   V = valid on this command.

13.0 ELECTRICAL SPECIFICATIONS

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias . . . . . -55°C to +125°C
Storage Temperature . . . . . -65°C to +150°C
D.C. Voltage on Pins[1] I3, I4, O4, and O5 to Ground Potential . . . . . -0.5V to V_{DD}+0.5V
Transient Voltage (<20 ns) on Pins[1] I3, I4, O4, and O5 to Ground Potential . . . . . -2.0V to V_{DD}+2.0V
D.C. Voltage on Pins[1] I1, I2, O1, O2, and O6 to Ground Potential. . . . . -0.5V to V_{DDQ}+0.5V
Transient Voltage (<20 ns) on Pins[1] I1, I2, O1, O2, and O6 to Ground Potential. . . . . -2.0V to V_{DDQ}+2.0V
Package Power Dissipation Capability (T_A = 25°C) 1.0W
Through Hole Lead Soldering Temperature (10 Seconds). . . . . 300°C
Surface Mount Solder Reflow Temperature . . . . . 260°C for 10 seconds
Output Short Circuit Current[2] . . . . . 50 mA

1. Please refer to Table 3-1 for pin assignment information.
2. Outputs shorted for no more than one second. No more than one output shorted at a time.

TABLE 13-1: Absolute Maximum Power Pin Stress Ratings

Parameter	Symbol	Conditions
Input Power	V_{DDQ} V_{DD}	-0.3V min to 6.5V max -0.3V min to 4.0V max
Voltage on any flash media interface pin with respect to V_{SS}		-0.5V min to V_{DD} + 0.5V max
Voltage on all other pins with respect to V_{SS}		-0.5V min to V_{DDQ} + 0.5V max

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Operating Range

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Commercial	0°C to +70°C	3.135-3.465V	4.5-5.5V; 3.135-3.465V
Industrial	-40°C to +85°C	3.135-3.465V	4.75-5.25V; 3.135-3.465V

AC Conditions of Test

Input Rise/Fall Time	10 ns
Output Load	C_L = 100 pF
See Figure 13-1	

Note: All AC specifications are guaranteed by design.

Advance Information

TABLE 13-2: Recommended System Power-on Timing

Symbol	Parameter	Typical	Maximum	Units
$T_{PU-INITIAL}$[1]	Drive Initialization to Ready	3 sec + (0.5 sec/ GByte)	100	sec
$T_{PU-READY1}$[2]	Host Power-on/Reset to Ready Operation	200	500	ms
$T_{PU-WRITE1}$[2]	Host Power-on/Reset to Write Operation	200	500	ms

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1. This parameter is only for expanded capacity option.
2. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 13-3: Capacitance (Ta = 25°C, f=1 MHz, other pins open)

Parameter	Description	Test Condition	Maximum
$C_{I/O}$[1]	I/O Pin Capacitance	$V_{I/O}$ = 0V	15 pF
C_{IN}[1]	Input Capacitance	V_{IN} = 0V	9 pF

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1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 13-4: Reliability Characteristics

Symbol	Parameter	Minimum Specification	Units	Test Method
I_{LTH}[1]	Latch Up	100 + I_{DD}	mA	JEDEC Standard 78

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1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

13.1 DC Characteristics

TABLE 13-5: DC Characteristics for Media Interface

Symbol	Type	Parameter	Min	Max	Units	Conditions
V_{IH3} V_{IL3}	I3	Input Voltage	2.0	 0.8	V	V_{DD}=V_{DD} Max V_{DD}=V_{DD} Min
I_{IL3}	I3Z	Input Leakage Current	-10	10	uA	V_{IN} = GND to V_{DD}, V_{DD} = V_{DD} Max
I_{U3}	I3U	Input Pull-Up Current	-8	-50	uA	V_{IN} = GND, V_{DD} = V_{DD} Max
I_{D3}	I3D	Input Pull-Down Current	30	200	uA	V_{IN} = V_{DD}, V_{DD} = V_{DD} Max
V_{T+4} V_{T-4}	I4	Input Voltage Schmitt Trigger	 0.75	2.5	V	V_{DD} = V_{DD} Max V_{DD} = V_{DD} Min
I_{IL4}	I4Z	Input Leakage Current	-10	10	uA	V_{IN} = GND to V_{DD}, V_{DD} = V_{DD} Max
I_{U4}	I4U	Input Pull-Up Current	-8	-50	uA	V_{IN} = GND, V_{DD} = V_{DD} Max
V_{OH4} V_{OL4}	O4	Output Voltage	2.4	 0.4	V	I_{OH4}=I_{OH4} Min I_{OL4}=I_{OL4} Max
I_{OH4}		Output Current	-1.5		mA	V_{DD}=V_{DD} Min
I_{OL4}		Output Current		1.5	mA	V_{DD}=V_{DD} Min
V_{OH5} V_{OL5}	O5	Output Voltage	2.4	 0.4	V	I_{OH5}=I_{OH5} Min I_{OL5}=I_{OL5} Max
I_{OH5}		Output Current	-3		mA	V_{DD}=V_{DD} Min
I_{OL5}		Output Current		3	mA	V_{DD}=V_{DD} Min

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TABLE 13-6: DC Characteristics for Host Interface

Symbol	Type	Parameter	Min	Max	Units	Conditions
V_{IH1} V_{IL1}	I1	Input Voltage	2.0V	 0.8V	V	V_{DDQ}=V_{DDQ} Max V_{DDQ}=V_{DDQ} Min
I_{IL1}	I1Z	Input Leakage Current	-10	10	uA	V_{IN} = GND to V_{DDQ}, V_{DDQ} = V_{DDQ} Max
I_{U1}	I1U	Input Pull-Up Current	-110	-1	uA	V_{OUT} = GND, V_{DDQ} = V_{DDQ} Max
V_{T+2} V_{T-2}	I2	Input Voltage Schmitt Trigger	 0.8	2.0	V	V_{DDQ}=V_{DDQ} Max V_{DDQ}=V_{DDQ} Min
I_{IL2}	I2Z	Input Leakage Current	-10	10	uA	V_{IN} = GND to V_{DDQ}, V_{DDQ} = V_{DDQ} Max
I_{U2}	I2U	Input Pull-Up Current	-110	-1	uA	V_{OUT} = GND, V_{DDQ} = V_{DDQ} Max
V_{OH1} V_{OL1}	O1	Output Voltage	2.4	 0.4	V	I_{OH1}=I_{OH1} Min I_{OL1}=I_{OL1} Max
I_{OH1}		Output Current	-4		mA	V_{DDQ}=V_{DDQ} Min
I_{OL1}		Output Current		4	mA	V_{DDQ}=V_{DDQ} Min
V_{OH2} V_{OL2}	O2	Output Voltage	2.4	 0.4	V	I_{OH2}=I_{OH2} Min I_{OL2}=I_{OL2} Max
I_{OH2}		Output Current	-6		mA	V_{DDQ}=3.135V-3.465V
I_{OL2}		Output Current		6	mA	V_{DDQ}=3.135V-3.465V
I_{OH2}		Output Current	-8		mA	V_{DDQ}=4.5V-5.5V
I_{OL2}		Output Current		8	mA	V_{DDQ}=4.5V-5.5V
V_{OH6} V_{OL6}	O6	Output Voltage for DASP# pin	2.4	 0.4	V	I_{OH6}=I_{OH6} Min I_{OL6}=I_{OL6} Max
I_{OH6}		Output Current for DASP# pin	-3		mA	V_{DDQ}=3.135V-3.465V
I_{OL6}		Output Current for DASP# pin		8	mA	V_{DDQ}=3.135V-3.465V
I_{OH6}		Output Current for DASP# pin	-3		mA	V_{DDQ}=4.5V-5.5V
I_{OL6}		Output Current for DASP# pin		12	mA	V_{DDQ}=4.5V-5.5V
I_{DD}[1,2]	PWR	Power supply current (T_A = 0°C to +70°C)		80	mA	V_{DD}=V_{DD} Max; V_{DDQ}=V_{DDQ} Max
I_{DD}[1,2]	PWR	Power supply current (T_A = -40°C to +85°C)		150	mA	V_{DD}=V_{DD} Max; V_{DDQ}=V_{DDQ} Max
I_{SP}	PWR	Sleep/Standby/Idle current (T_A = 0°C to +70°C)		150	µA	V_{DD}=V_{DD} Max; V_{DDQ}=V_{DDQ} Max
I_{SP}	PWR	Sleep/Standby/Idle current (T_A = -40°C to +85°C)		250	µA	V_{DD}=V_{DD} Max; V_{DDQ}=V_{DDQ} Max

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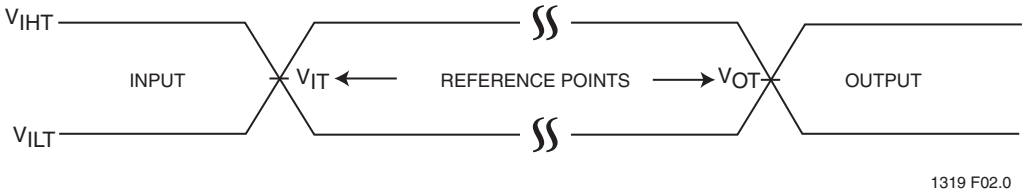
1. Sequential data transfer for 1 sector read data from host interface and write data to media.
2. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

13.2 AC Characteristics



AC test inputs are driven at V_{IHT} (0.9 V_{DD}) for a logic "1" and V_{ILT} (0.1 V_{DD}) for a logic "0". Measurement reference points for inputs and outputs are V_{IT} (0.5 V_{DD}) and V_{OT} (0.5 V_{DD}). Input rise and fall times (10% ↔ 90%) are <10 ns.

Note: V_{IT} - V_{INPUT} Test
V_{OT} - V_{OUTPUT} Test
V_{IHT} - V_{INPUT} HIGH Test
V_{ILT} - V_{INPUT} LOW Test

FIGURE 13-1: AC Input/Output Reference Waveforms

13.2.1 Host Side Interface I/O Input (Read) Timing Specification

TABLE 13-7: Host Side Interface I/O Read Timing

Symbol	Parameter	Min	Max	Units
T_{SU} (IORD#)	Data Setup before IORD#	20	-	ns
T_H (IORD#)	Data Hold following IORD#	5	-	ns
T_W (IORD#)	IORD# Width Time	70	-	ns
T_{SUA} (IORD#)	Address Setup before IORD#	25	-	ns
T_{HA} (IORD#)	Address Hold following IORD#	10	-	ns
T_{DF} IOCS16#(ADR)	IOCS16# Delay Falling from Address	-	20	ns
T_{DR} IOCS16#(ADR)	IOCS16# Delay Rising from Address	-	20	ns

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Note: The maximum load on IOCS16# is 1 LSTTL with 50pF total load.
All AC specifications are guaranteed by design.

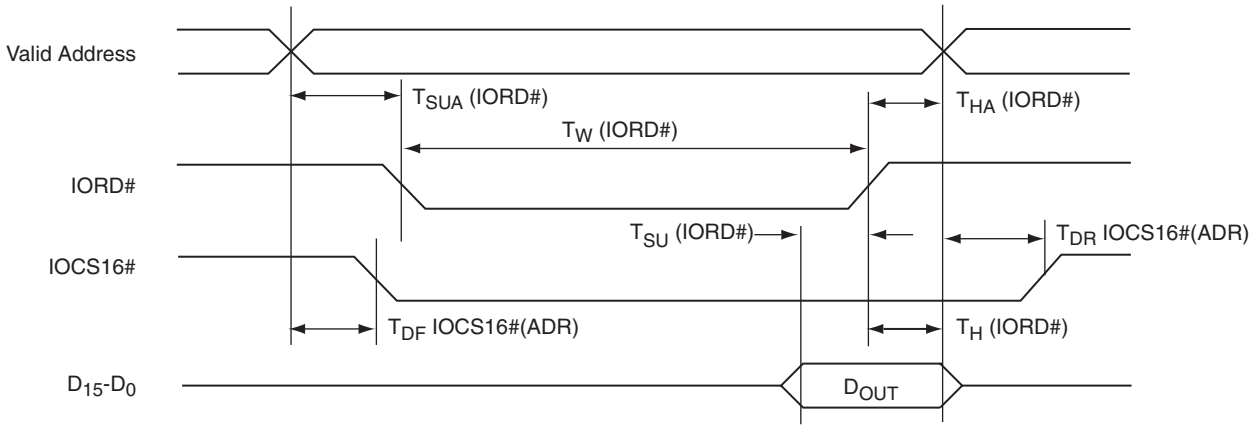

FIGURE 13-2: Host Side Interface I/O Read Timing Diagram

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13.2.2 Host Side Interface I/O Output (Write) Timing Specification

TABLE 13-8: Host Side Interface I/O Write Timing Specification

Symbol	Parameter	Min	Max	Units
T_{SU} (IOWR#)	Data Setup before IOWR#	20	-	ns
T_H (IOWR#)	Data Hold following IOWR#	10	-	ns
T_W (IOWR#)	IOWR# Width Time	70	-	ns
T_{SUA} (IOWR#)	Address Setup before IOWR#	25	-	ns
T_{HA} (IOWR#)	Address Hold following IOWR#	10	-	ns
T_{DF} IOCS16#(ADR)	IOCS16# Delay Falling from Address	-	20	ns
T_{DR} IOCS16#(ADR)	IOCS16# Delay Rising from Address	-	20	ns

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Note: The maximum load on IOCS16# is 1 LSTTL with 50pF total load.
All AC specifications are guaranteed by design.

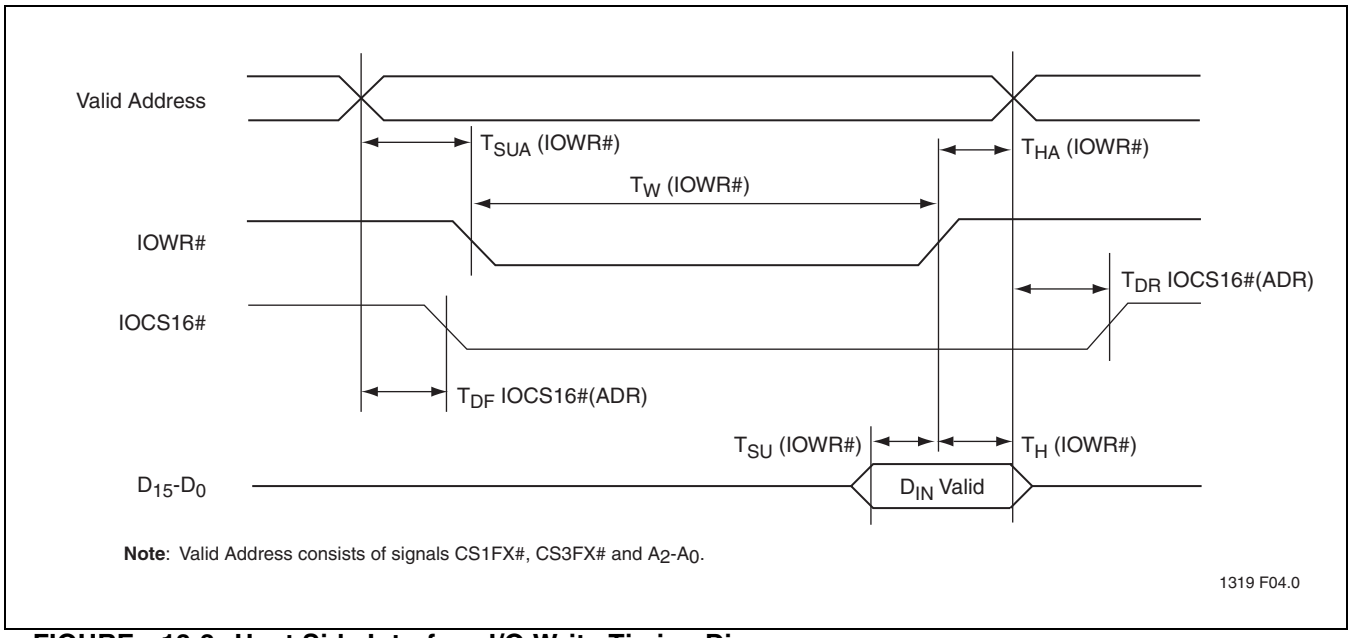

FIGURE 13-3: Host Side Interface I/O Write Timing Diagram

13.2.3 Multi-word DMA Data Transfer

TABLE 13-9: Multi-word DMA Timing Parameters - Mode 2

Symbol	Parameter	Min	Max	Units
T_0[1]	Cycle Time	120		ns
T_D	IORD#/IOWD# Asserted Pulse Width	70		ns
T_E	IORD# Data Access		50	ns
T_F	IORD# Data Hold	5		ns
T_G	IORD#/IOWD# Data Setup	20		ns
T_H	IOWD# Data Hold	10		ns
T_I	DMACK# to IORD#/IOWR# Setup	0		ns
T_J	IORD#/IOWD# to DMACK Hold	5		ns
T_{KR}	IORD# Negated Pulse Width	25		ns
T_{KW}	IOWD# Negated Pulse Width	25		ns
T_{LR}	IORD# to DMARQ Delay		35	ns
T_{LW}	IOWD# to DMARQ Delay		35	ns
T_M	CS(1:0) Valid to IORD#/IOWD#	25		ns
T_N	CS(1:0) Hold	10		ns
T_Z	DMACK# to Read Data Released		25	ns

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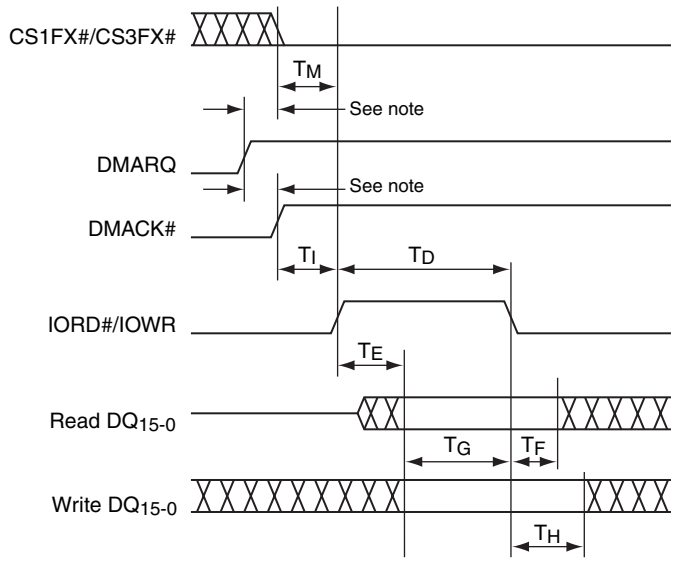
1. T_0 is the minimum total cycle time, T_D is the minimum IORD#/IOWD# assertion time, and T_K (T_{KR} or T_{KW}, as appropriate) is the minimum IORD#/IOWD# negation time. A host should lengthen T_D and/or T_K to ensure that T_0 is equal to the value reported in the device ID.

Note: All AC specifications are guaranteed by design.



Note: The host should not assert DMACK# or negate both CS1FX# and CS3FX# until the assertion of DMARQ is detected. The maximum time from the assertion of DMARQ to the assertion of DMACK# or the negation of both CS0 and CS1 is not defined.

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FIGURE 13-4: Initiating a Multi-word DMA Data Transfer

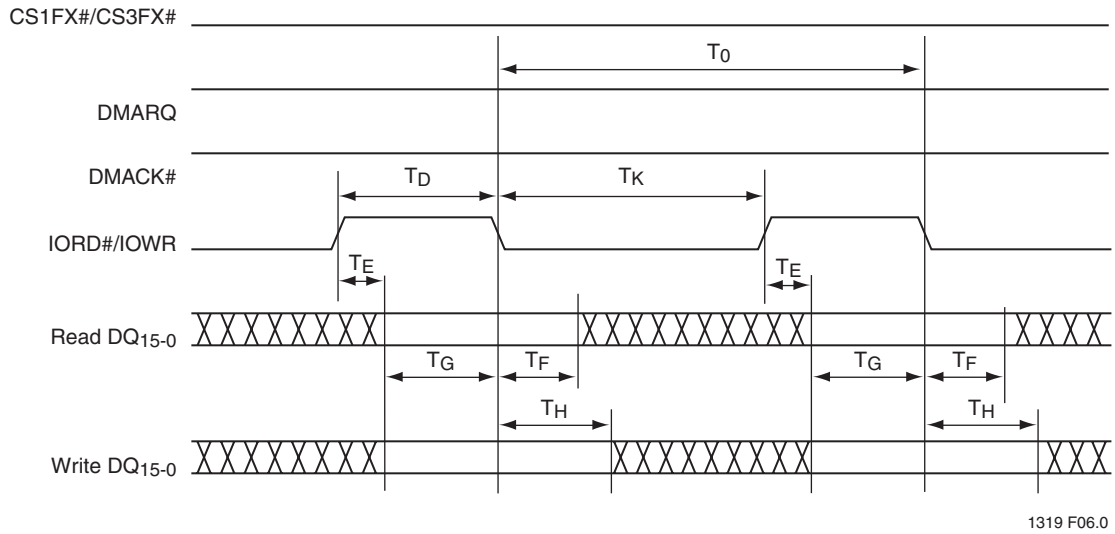
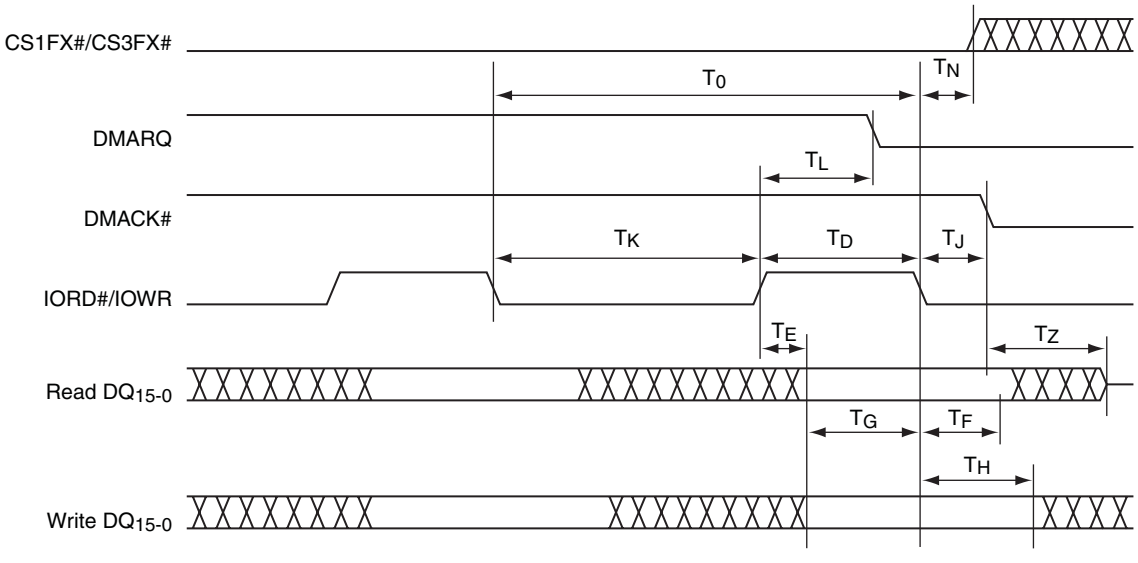
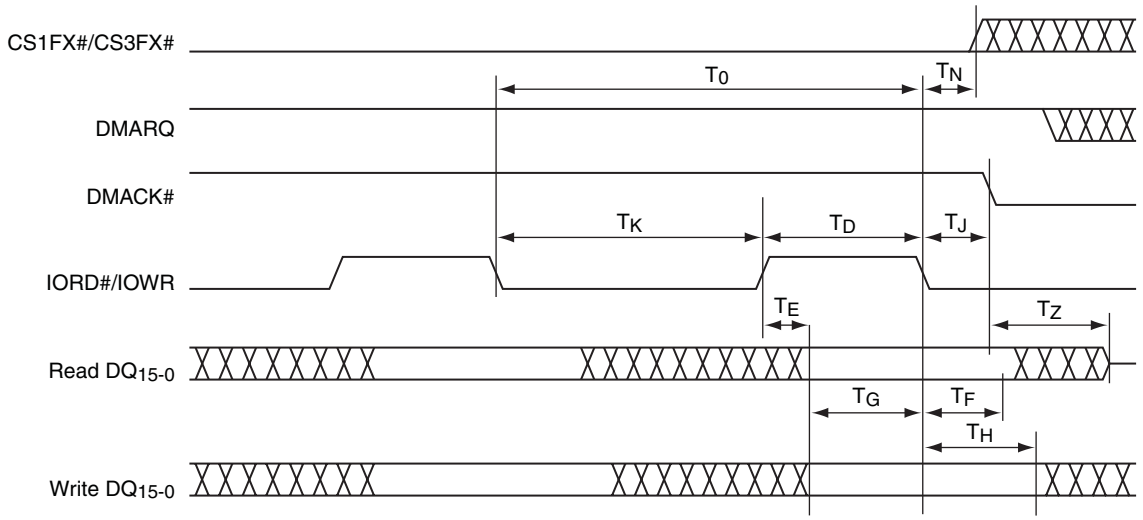


FIGURE 13-5: Sustaining a Multi-word DMA Data Transfer



Note: To terminate the data burst, the Device shall negate DMARQ within the T_L of the assertion of the current IORD# or IOWR# pulse. The last data word for the burst should be transferred by the negation of the current IORD# or IOWR# pulse. If all data for the command has not been transferred, the device shall reassert DMARQ again at any later time to resume the DMA operation.

FIGURE 13-6: Device Terminates a Multi-word DMA Data Transfer



Note: 1. To terminate the transmission of a data burst, the host should negate DMACK# within the specified time after a IORD# or IOWR# pulse. No further IORD# or IOWR# pulses shall be asserted for this burst.
2. If the device is able to continue the transfer of data, the device may leave DMARQ asserted and wait for the host to reassert DMACK# or may negate DMARQ at any time after detecting that DMACK# has been negated.

1319 F08.0

FIGURE 13-7: Host Terminates a Multi-word DMA Data Transfer

13.2.4 External Flash Media Bus I/O Timing Specifications

TABLE 13-10: External Flash Media Bus Timing Parameters

Symbol	Parameter	Min	Max	Units
T_{CLS}	FCLE Setup Time	20	-	ns
T_{CLH}	FCLE Hold Time	40	-	ns
T_{CS}	FCE# Setup Time	40	-	ns
T_{CH}	FCE# Hold Time for Command/Data Write Cycle	40	-	ns
T_{CHR}	FCE# Hold Time for Sequential Read Last Cycle	-	40	ns
T_{WP}	FWE# Pulse Width	20	-	ns
T_{WH}	FWE# High Hold Time	20	-	ns
T_{WC}	Write Cycle Time	40	-	ns
T_{ALS}	FALE Setup Time	20	-	ns
T_{ALH}	FALE Hold Time	40	-	ns
T_{DS}	FAD[15:0] Setup Time	20	-	ns
T_{DH}	FAD[15:0] Hold Time	20	-	ns
T_{RP}	FRE# Pulse Width	20	-	ns
T_{RR}	Ready to FRE# Low	40	-	ns
T_{REA}	FRE# Data Setup Access Time	20	-	ns
T_{RC}	Read Cycle Time	40	-	ns
T_{REH}	FRE# High Hold Time	30	-	ns
T_{RHZ}	FRE# High to Data Hi-Z	5	-	ns

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Note: All AC specifications are guaranteed by design.

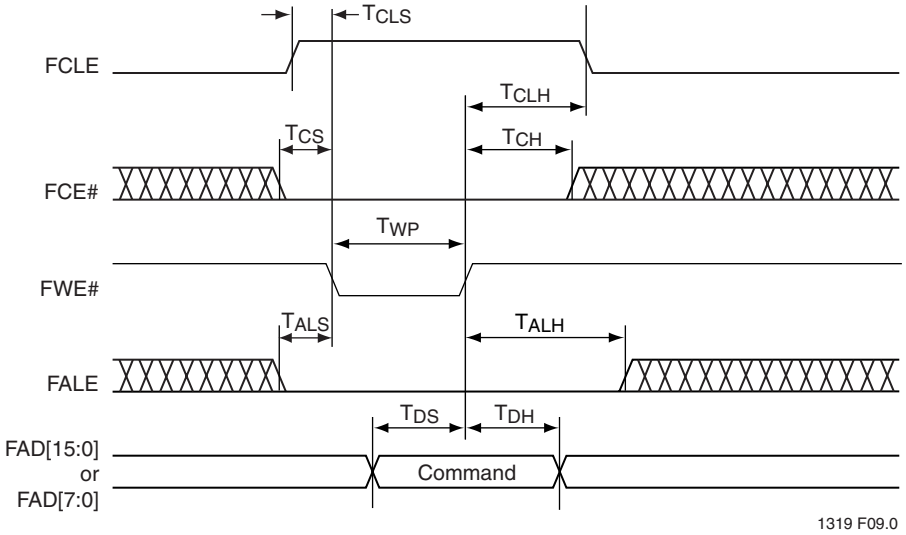

FIGURE 13-8: Media Command Latch Cycle

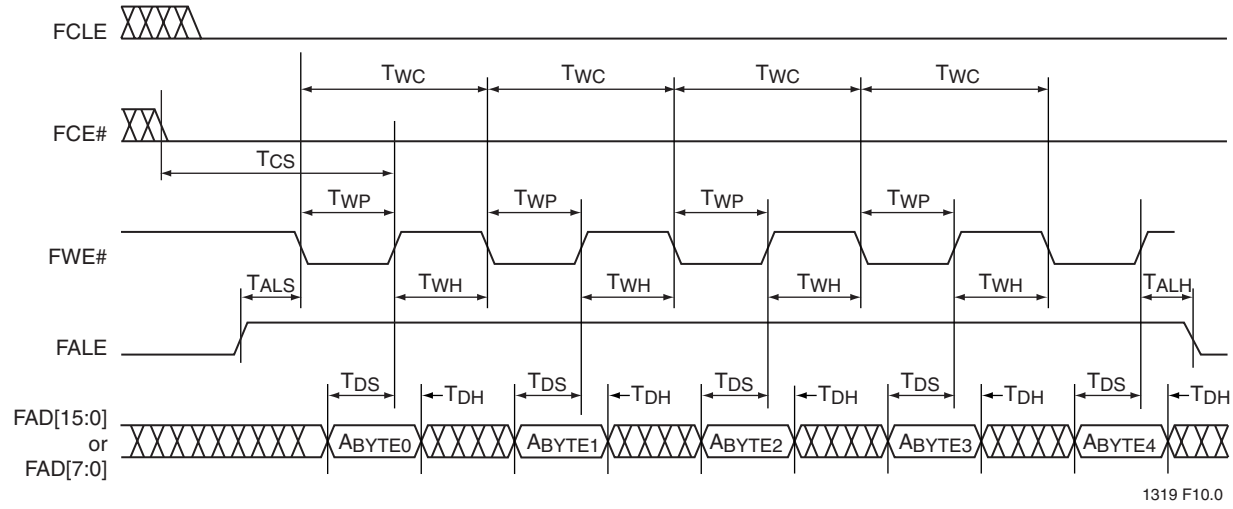

FIGURE 13-9: Media Address Latch Cycle

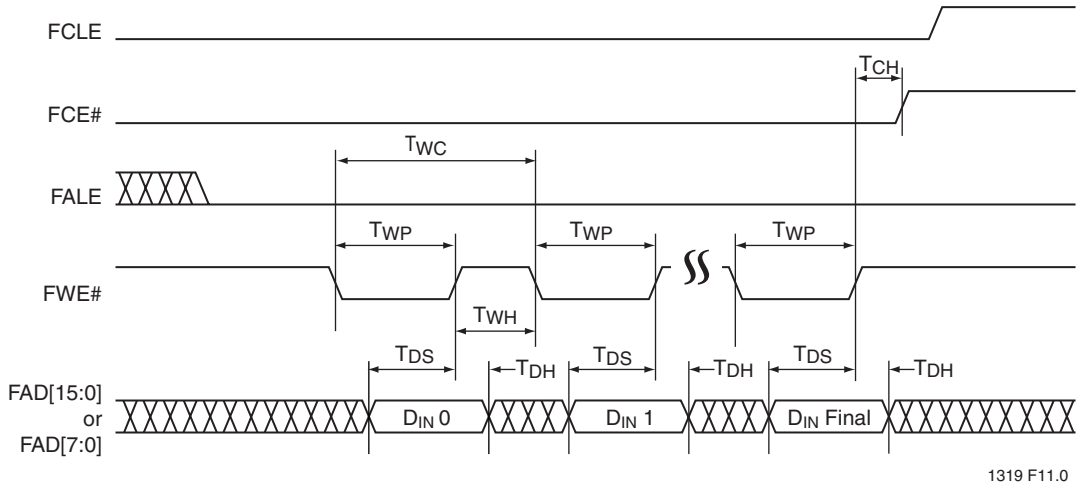

FIGURE 13-10: Media Data Loading Latch Cycle

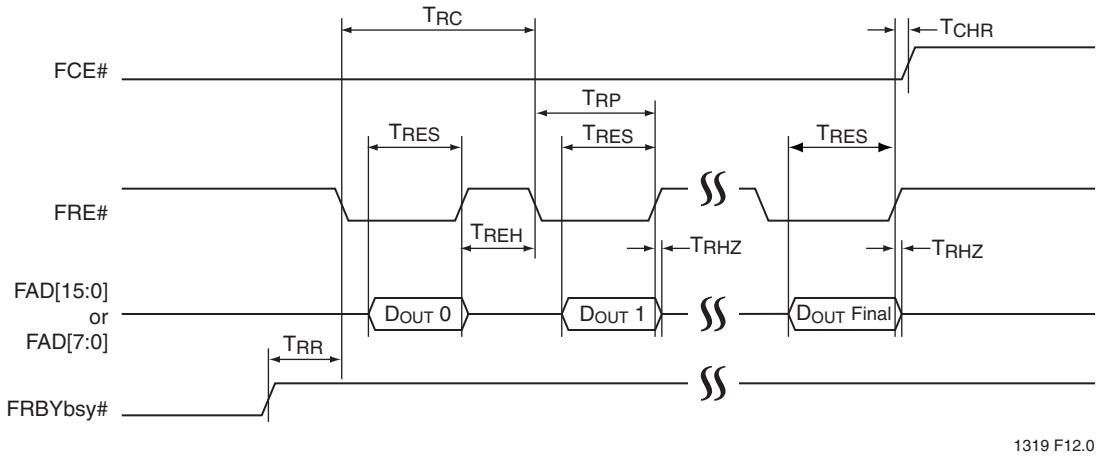

FIGURE 13-11: Media Data Read Cycle

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14.0 APPENDIX

14.1 Differences between the SST NANDrive IC and ATA/ATAPI-5 Specifications

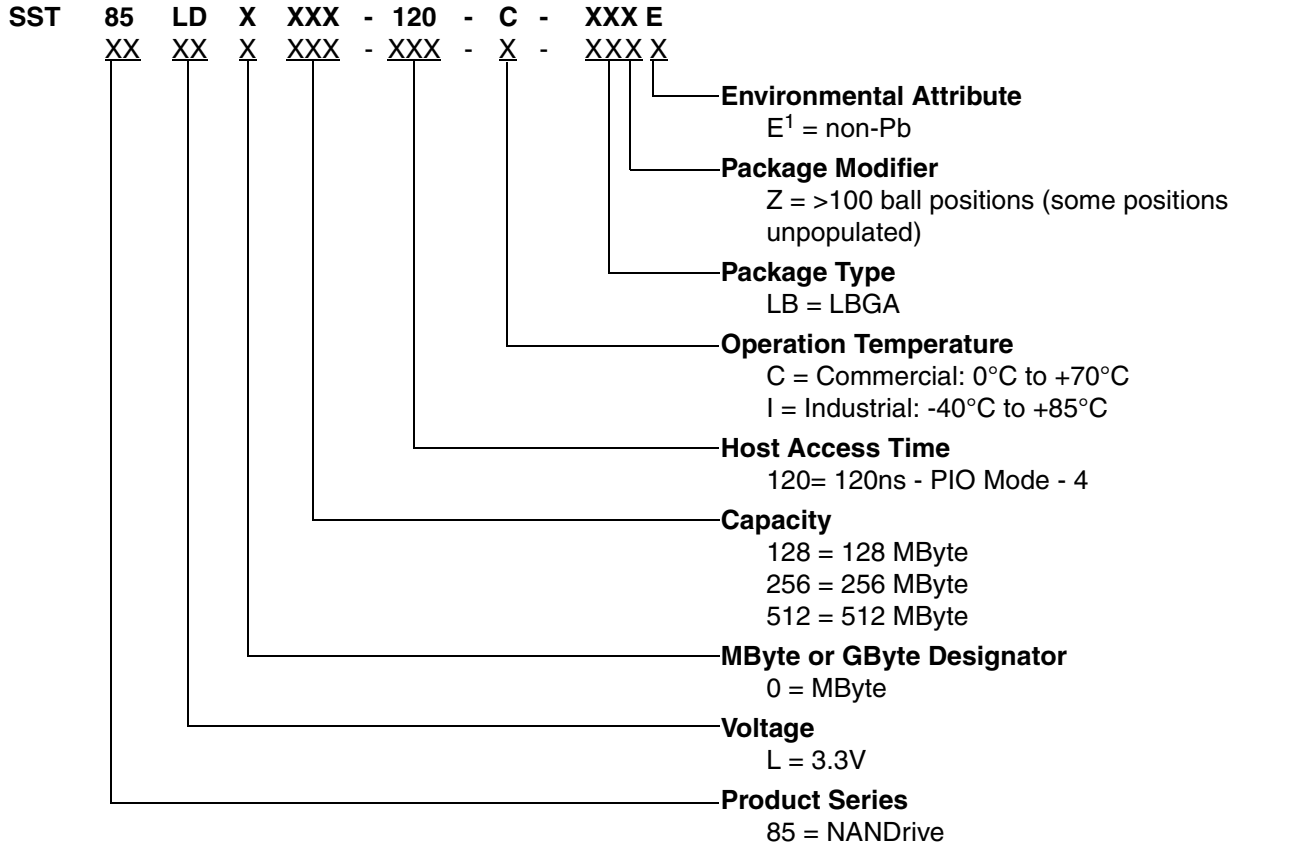
14.1.1 Idle Timer

The Idle timer uses an incremental value of 5 ms, rather than the 5 sec minimum increment value specified in ATA specifications.

14.1.2 Recovery from Sleep Mode

For NANDrive devices, recovery from sleep mode is accomplished by simply issuing another command to the device. A hardware or software reset is not required.

15.0 PRODUCT ORDERING INFORMATION



1 Environmental suffix “E” denotes non-Pb solder.
SST non-Pb solder devices are “RoHS Compliant”.

15.1 Valid Combinations

SST85LD0128-120-C-LBZE	SST85LD0256-120-C-LBZE	SST85LD0512-120-C-LBZE
SST85LD0128-120-I-LBZE	SST85LD0256-120-I-LBZE	SST85LD0512-120-I-LBZE

Note: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

16.0 PACKAGING DIAGRAM

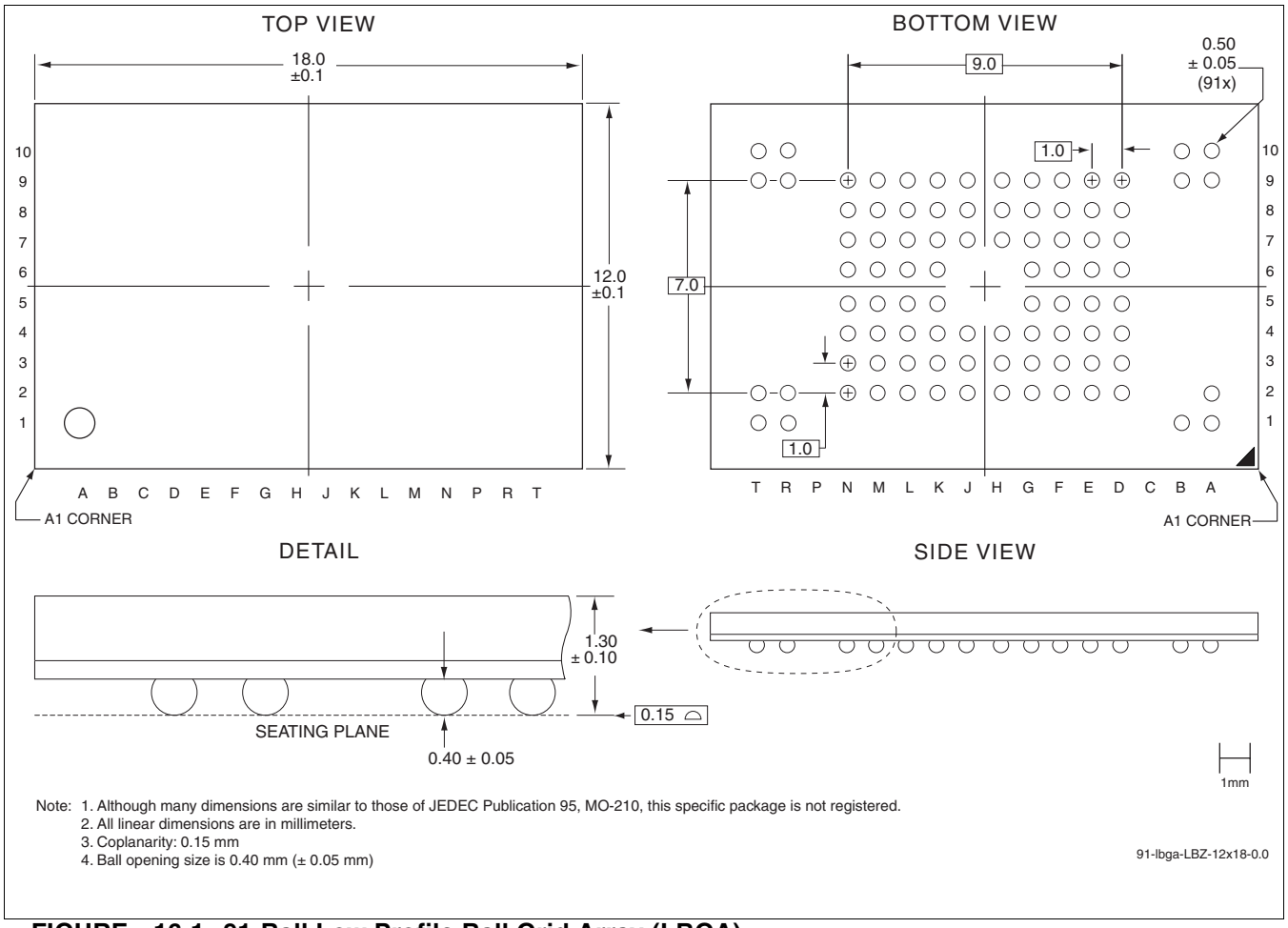


FIGURE 16-1: 91-Ball Low Profile Ball Grid Array (LBGA)
SST Package Code: LBZ

TABLE 16-1: Revision History

Number	Description	Date
00	• Initial release	Aug 2006
01	• Changed Package Code from LBS to LBZ on pages 71 and 72 • Edited Table 3-1 on page 10. Changed VREG cross-reference from footnote 2 to footnote 1. Assigned footnote 2 to DNU. In VREG Name and Function, changed 0.1µ to 4.7µ. • Edited Table 12-4. Changed Word 21 Default Value from 0200h to 0002H. • Edited Table 12-4 on pages 24 and 25. Removed footnotes 3 through 6 and reassigned footnotes 1 and 2 throughout the table. • Edited Section 12.2.1.6.6 Word 10-19 Serial Number description on page 25 • Replaced SS755LD019x with NANDrive on page 28 • Changed Operating Range for Commercial and Industrial VDD and VDDQ from 3.165V to 3.135V	Nov 2006
02	• Edited the Pin Assignment Figure 3-1 and Table 3-1 to include all NC pins.	Dec 2006
03	• Added SST85LF0256 and SST85LD0512 globally. • Edited Figure 3-1 and Figure 16-1 to replace “S” with “T”. • Edited Table 4-1: removed all but 128, 256, and 512 MB capacity settings. • Edited Active and Sleep mode parameters in the Features on page 1. • Added Table 4-2 Sustained Performance on page 11.	Feb 2007